CMS32M57xx Datasheet

ARM® Cortex® -M0 32-bit microcontroller

Rev. 1.0.7

1. Product characteristics

1.1 MCU function&feature

- **Internal ARM Cortex™-M0, 64MHz@2.1V~5.5V**
  - Single-cycle 32-bit hardware multiplier
- **32-bit hardware divider (HWDIV)**
  - Signed/unsigned mode, complete the operation with 6 HCLKs
- **Memory**
  - Max. 64KB programmable FLASH (APROM+BOOT)
  - 1KB FLASH data area (seperated space)
  - Max. 8KB SRAM (Support partition write protection function)
  - Support BOOT function, BOOT can be set to 0-4KB
  - Support hardware CRC to check FLASH space code
  - Support FLASH partition protection (min. unit of 2KB)
- **System clock**
  - Internal high-speed oscillation 48MHz/64MHz (HSI)
  - Internal low-speed oscillation 40KHz (LSI)
- **GPIO (max. of 46 I/Os)**
- **LVR (1.9V/2.1V/2.6V)**
- **LVD (2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.2V)**
- **Built-in temperature sensor (TS)**
- **System timer**
  - 24-bit SysTick timer
  - Watchdog timer (WDT)
  - Window watchdog timer (WWDT)
- **Normal mode/sleep mode/deep sleep mode/stop mode**
- **Cyclic redundancy check (CRC)**
- **Timer (32bit/16bit-TIMER0/1/2/3)**
- **Capture/compare/pulse width modulation (CCP0/1)**
  - Support 4 channels of simultaneous capture, can be connected to the Hall sensor interface
- **Communication port**
  - 1 I^2C module (max. speed 1Mb/s)
- **Enhanced PWM (EPWM)**
  - 6 channels and channels can be remapeped
  - Support independent/complementary/synchronous /group output mode
  - Support edge/center alignment counting mode
  - Support single/continuous/interval loading update mode
  - Support complementary mode to insert dead zone delay
  - Support mask and mask preset (a total of 8 mask state buffers)
  - Support Hall sensor interface (hardware control PWM output)
  - Support fault protection and 6 sorts of brake signal sources
  - Support 4 software/hardware failure recovery modes
- **ADC0 (12bit, 100Ksps)**
  - Max. of 20 channels
  - Each conversion channel has an independent result register
  - Support single/continuous mode
  - Supports 2 hardware trigger modes, 9 trigger sources in total
  - 1 conversion result comparator which can generate interrupt
- **ADCB (12bit, 1.2Msps)**
  - Max. of 20 channels
  - Each conversion channel has an independent result register
  - Support single/continuous/insert mode
  - Supports 5 hardware trigger modes, 17 trigger
  - sources in total
  - 1 conversion result comparator which can generate
  - interrupt
- **Analog comparator (ACMP0/1)**
  - 4 options for positive side, internal 1.2V/VDD voltage divider for negative side

- 1 SSP/SPI module (adjustable 4-16 bit data format)
- Max. of 2 UART：UART0/1 (total of 32 receive/send FIFO)

◆ **Serial wire debug SWD (2-Wire)**

◆ **96bit unique ID (UID)**

◆ **128bit user UID (USRUID)**

- User can set, can be encrypted (can be used as a security key)
- Support single/double hysteresis voltage selection：10mV/20mV/60mV
- Support comparator output to trigger EPWM brake

◆ **Programmable gain amplifier (PGA0/1)**

- 2 choices on positive end
- The output can be connected to the input of the internal ADC channel and the analog comparator
- Internal gain can be selected from: 4 times ~ 32 times

◆ **Operational Amplifier (OP0/1)**

- Input can be connected to internal 1.2V reference
- The output can be connected to the input of the internal ADC channel and the analog comparator
- Can be set to comparator mode

◆ **Support safety-related functions and applications**

- Meet IEC60730 CLASS B standard

1.2 Product comparison

Peripheral interface \ Product name		CMS32M5710L048	CMS32M5733Q048	CMS32M5736L048	CMS32M5736Q048
Built-in drive supply voltage		-	5.5~18V	8~20V	
GATE DRIVER		-	6N	6N	
MCU Operating Voltage		2.1V~5.5V			
Maximum clock frequency		64MHz			
Storage module	APROM	60/62/63/64KB (1)			
	BOOT	0/1/2/4KB (1)			
	Data FLASH	1KB			
	SRAM	8KB			
Timer	SysTick	1(24-bit)			
	WDT	1			
	WWDT	1			
	TIMER0/1/2/3	4(16/32-bit)			
Enhanced Digital peripherals	CRC	CRC16-CCITT			
	Divider	32 / 32 bit			
	CCP	2	2	2	2
	EPWM	6(16-bit)			
Communication port	UART	2			
	I2C	1			
	SSP/SPI	1			
Analog module	12bit-ADC0 (number of channels)	12ext chs +8spc chs (2)	11ext chs +8spc chs (2)	11ext chs +8spc chs (2)	11ext chs +8spc chs (2)
	12bit-ADCB (number of channels)	12ext chs +8spc chs (2)	12ext chs +8spc chs (2)	12ext chs +8spc chs (2)	12ext chs +8spc chs (2)
	ACMP	2			
	OP	2			
	PGA	2			
	Temperature sensor (TS)	1			
GPIOs		46	32	32	32
LVR		1.9V/2.1V/2.6V			
LVD		2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.2V			
Operating temperature		-40℃~105℃			
Encapsulation		LQFP48	QFN48	LQFP48	QFN48

Note：

1) Set the size of APROM and BOOT space through the system configuration register, the maximum space of APROM and BOOT in total is 64KB.

2) ADC0/ADCB has up to 12 external channels and 8 dedicated channels (output port of OP0/1, output port of PGA0/1, temperature sensor, internal reference, ADC reference positive/negative terminal, etc.).

3) Indicates the number of analog modules. The analog function is not realized through the input/output of the pins. Theinput/output pins are subject to the actual product.

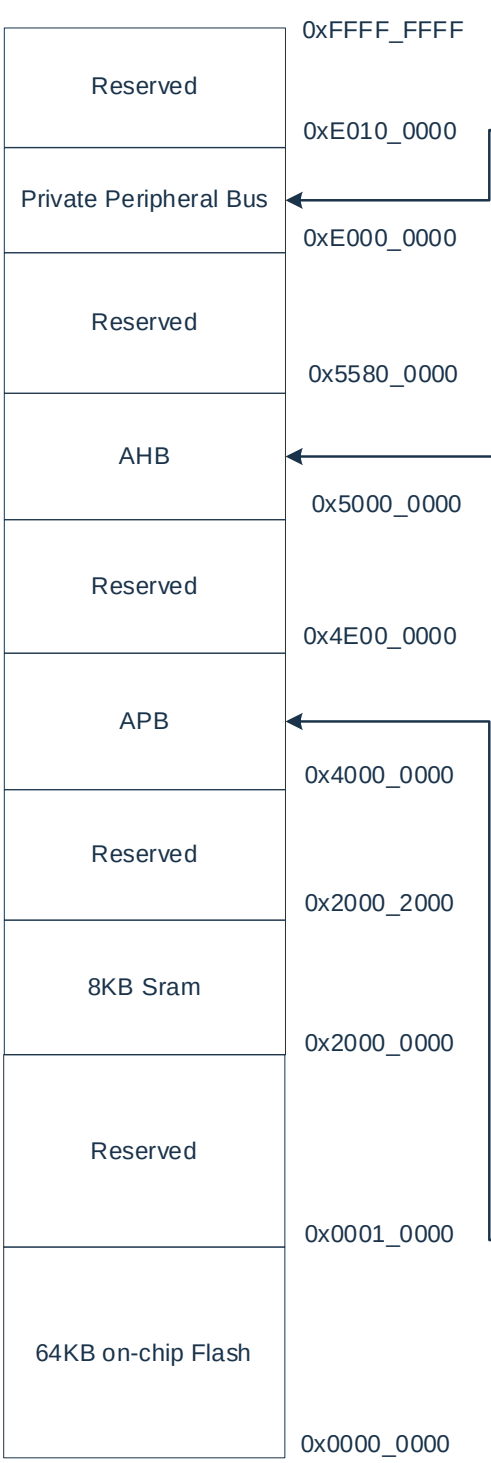
2. System overview

2.1 System introduction

This series of products integrates the ARM® Cortex®-M0 core and a built-in nested vector interrupt controller. There are mainly parallel I/O ports (supporting normal input, pull-up and pull-down input, push-pull output, open-drain output, and can be configured with edge or level trigger interrupts), timer (6-bit window watchdog timer, 32-bit watchdog timer, 4-channel programmable timer), SPI, I2C, UART, EPWM, CCP, ADC, ACMP, O P, PGA and other components. The main features are as follows:

- It has a maximum of 64KB FLASH storage space, a maximum of 8KB SRAM space, and 1KB FLASH data area.
- Higher security: support BOOT function and program space partition protection, support hardware CRC check FLASH space code, register protection operation, user configurable ID.
- Four working modes are available: normal mode, sleep mode, deep sleep mode, and stop mode, which are more convenient to use and lower power consumption.
- With 32-bit hardware divider and 32-bit single-cycle hardware multiplier, the operation speed is faster.
- The flexible and configurable IO port supports a variety of digital and analog multiplexing functions, making it more convenient to use.
- It has enhanced PWM with dead zone programming, periodic duty cycle interval update, independent/ complementary/ synchronous/ master control output, multiple fault protection functions, and support for software/hardware recovery functions. EPWM functions are more abundant.
- With 12-bit ADC with the fastest 1.2Msps, analog comparators that support hysteresis selection, programmable gain amplifiers with selectable gains, operational amplifiers and other analog IPs, the analog functions are more powerful.

2.2 Memory mapping



Private Peripheral Bus

Nested Vectored Interruput Controlle	0xE000_EF00
System Control Block	0xE000_ED00
Nested Vectored Interruput Controlle	0xE000_E100
SysTick System Timer	0xE000_E010
System Control Block	0xE000_E008

AHB Bus

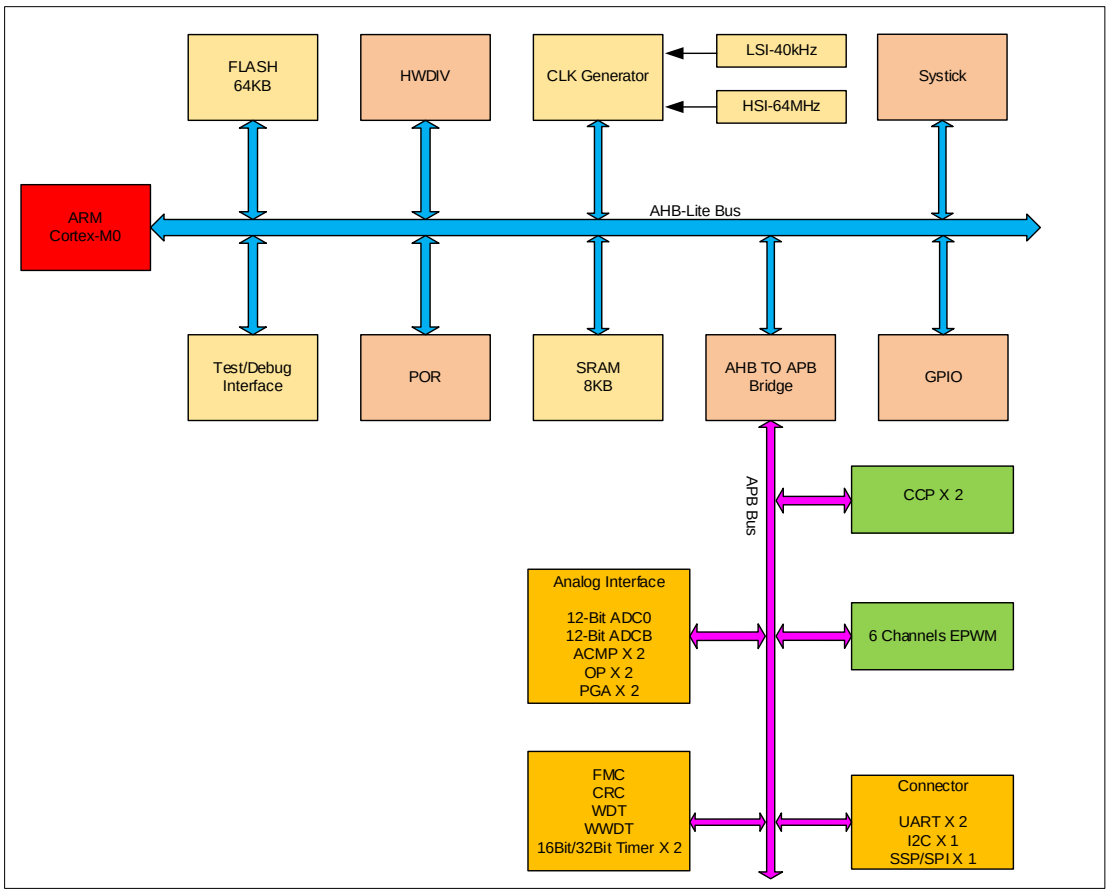
HWDIV Control	0x5500_0000
GPIO5 Control	0x5480_0000
GPIO4 Control	0x5400_0000
GPIO3 Control	0x5380_0000
GPIO2 Control	0x5300_0000
GPIO1 Control	0x5280_0000
GPIO0 Control	0x5200_0000
Reserved	0x5180_0000
Reserved	0x5100_0000
Reserved	0x5080_0000
System Configuration	0x5000_0000

APB Bus

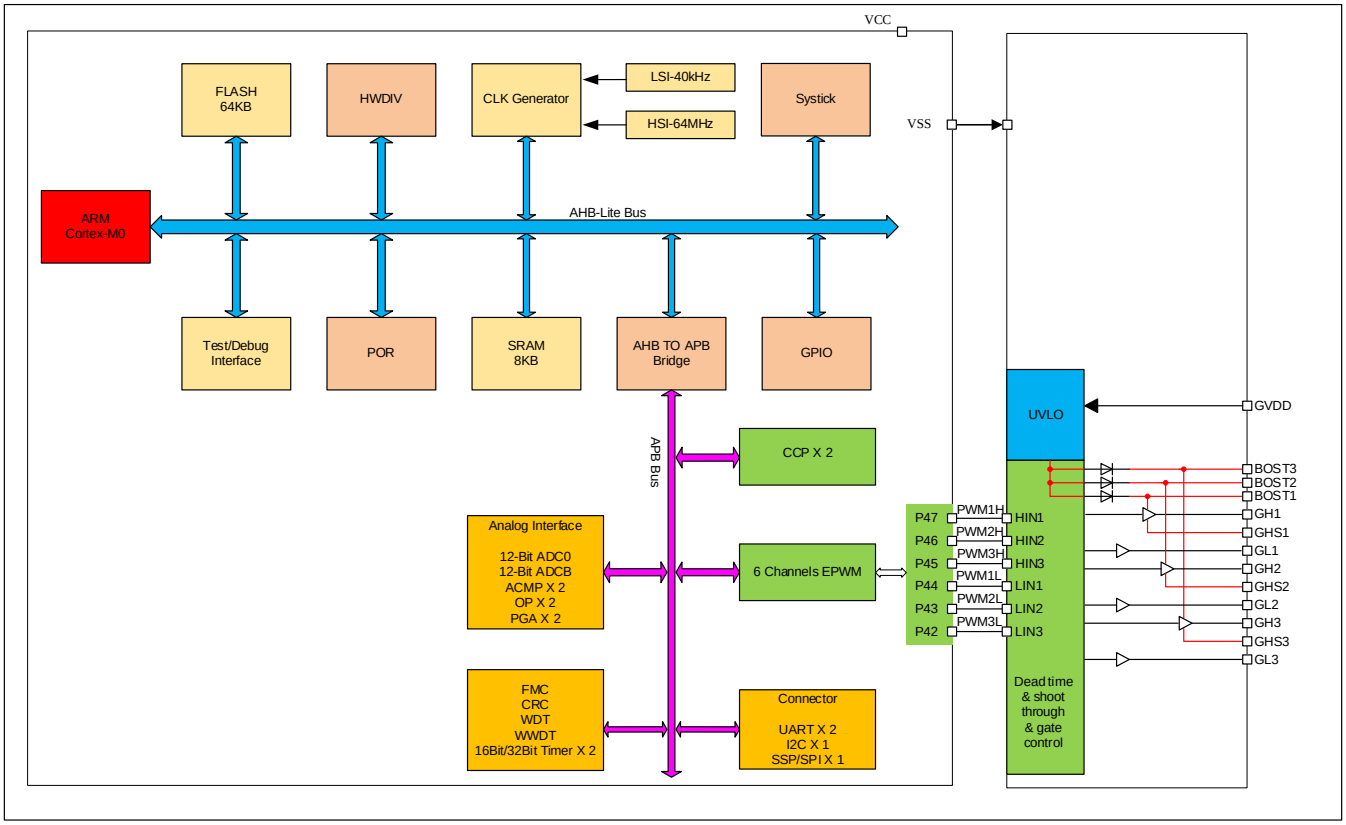
ADCB Control	0x4D80_0000
ACMP Control	0x4D00_0000
OP/PGA Control	0x4C80_0000
Reserved	0x4C00_0000
Reserved	0x4B80_0000
Reserved	0x4B00_0000
EPWM Control	0x4A80_0000
CRC Control	0x4A00_0000
FMC Control	0x4980_0000
Reserved	0x4900_0000
Reserved	0x4880_0000
I2C Control	0x4800_0000
WDT Control	0x4780_0000
TIMER2/3 Control	0x4700_0000
TIMER0/1 Control	0x4680_0000
Reserved	0x4600_0000
Reserved	0x4580_0000
UART1 Control	0x4500_0000
UART0 Control	0x4480_0000
Reserved	0x4400_0000
SSP/SPI Control	0x4380_0000
ADC0 Control	0x4300_0000
CCP Control	0x4280_0000
Reserved	0x4200_0000
WWDT Control	0x4180_0000
Reserved	0x4100_0000
Reserved	0x4080_0000
Reserved	0x4000_0000

2.3 System block diagram

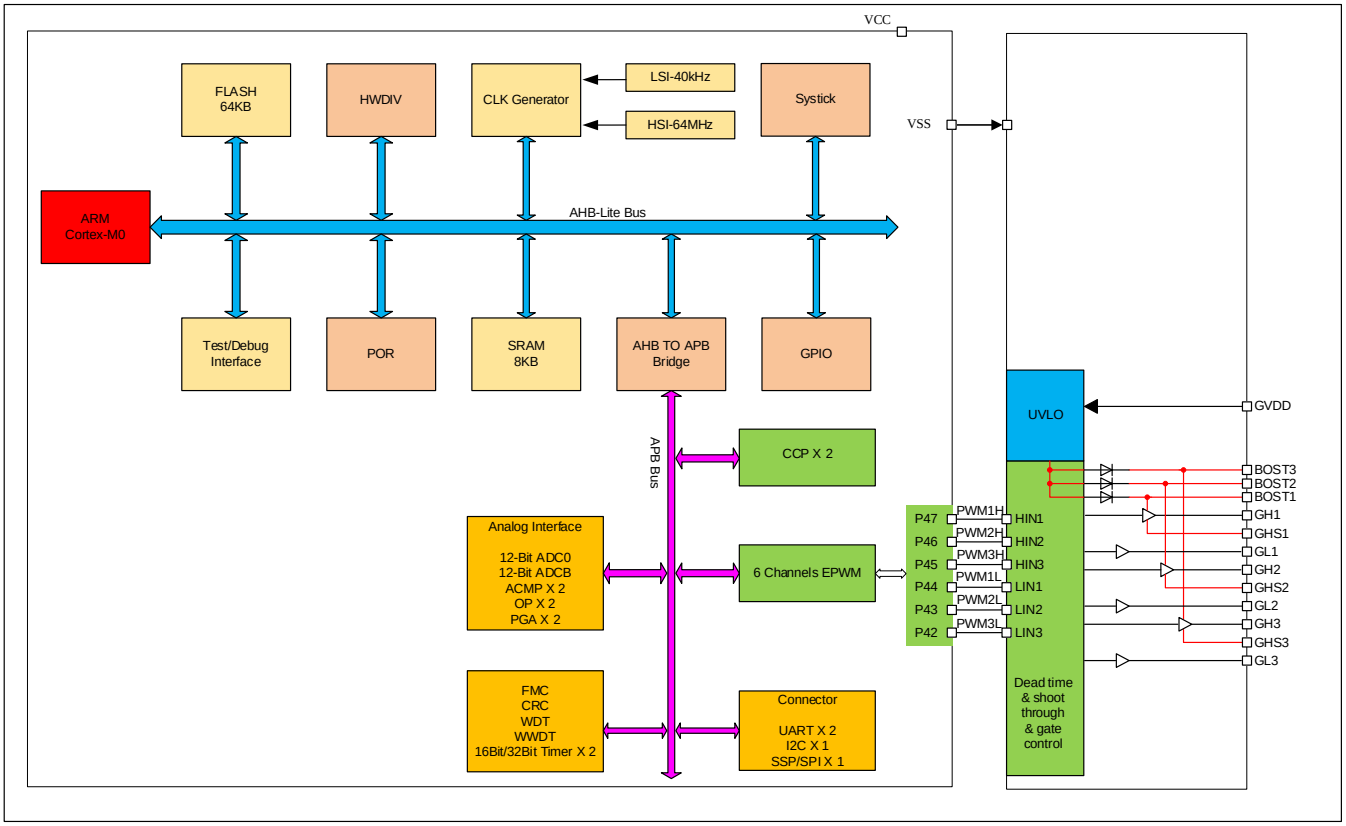
2.3.1 CMS32M5710 (LQFP48)



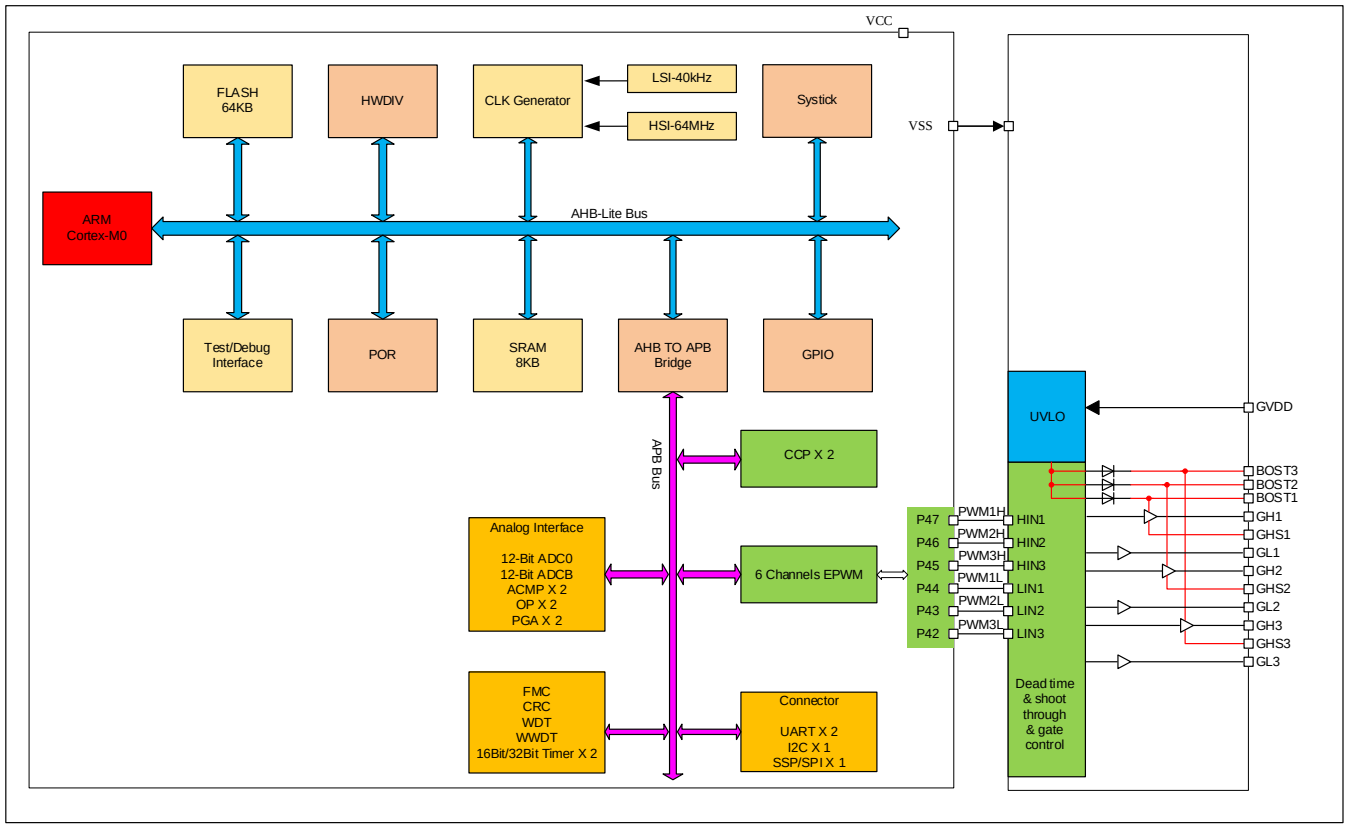
2.3.2 CMS32M5733 (QFN48)



2.3.3 CMS32M5736（LQFP48）



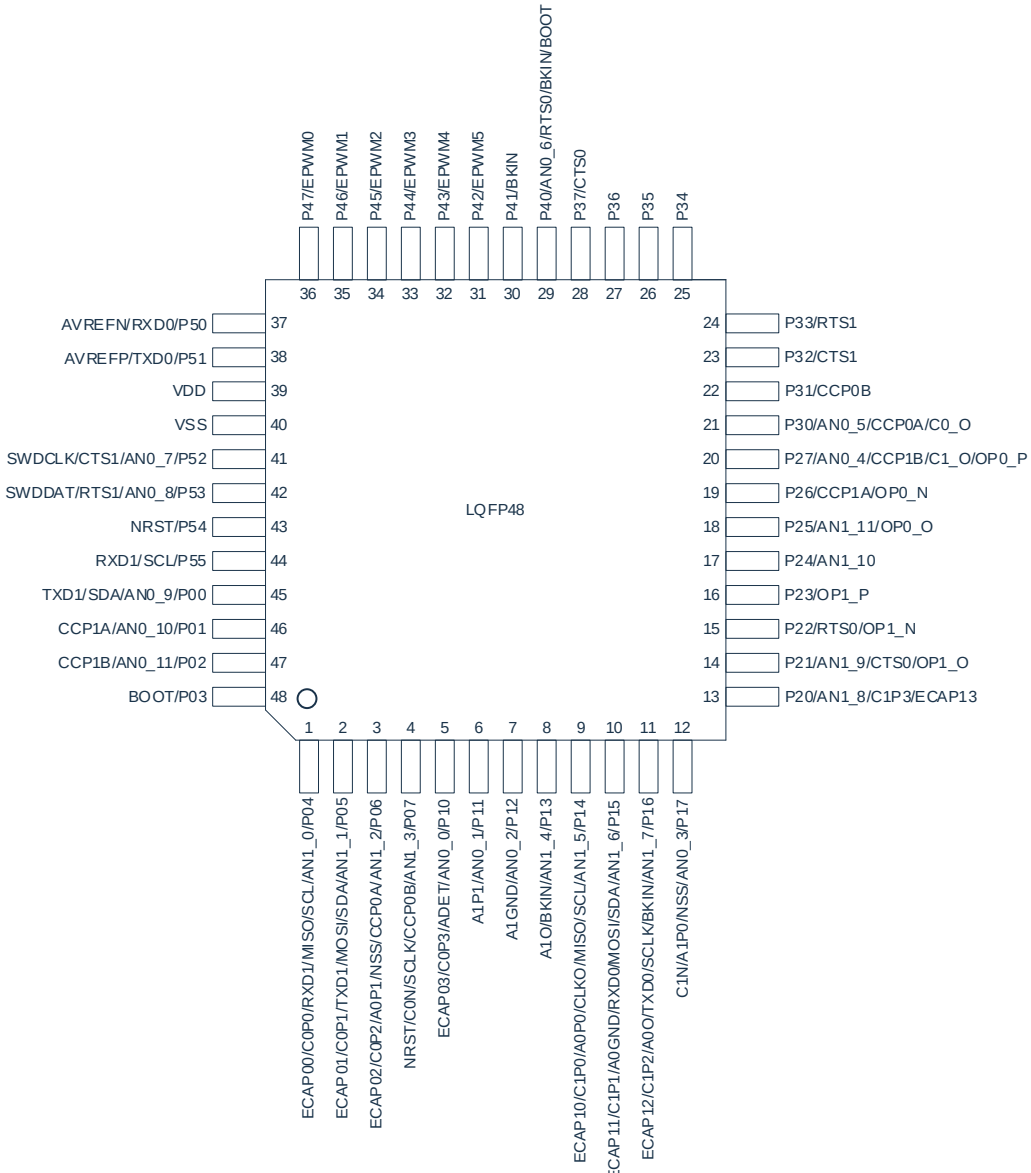
2.3.4 CMS32M5736 (QFN48)



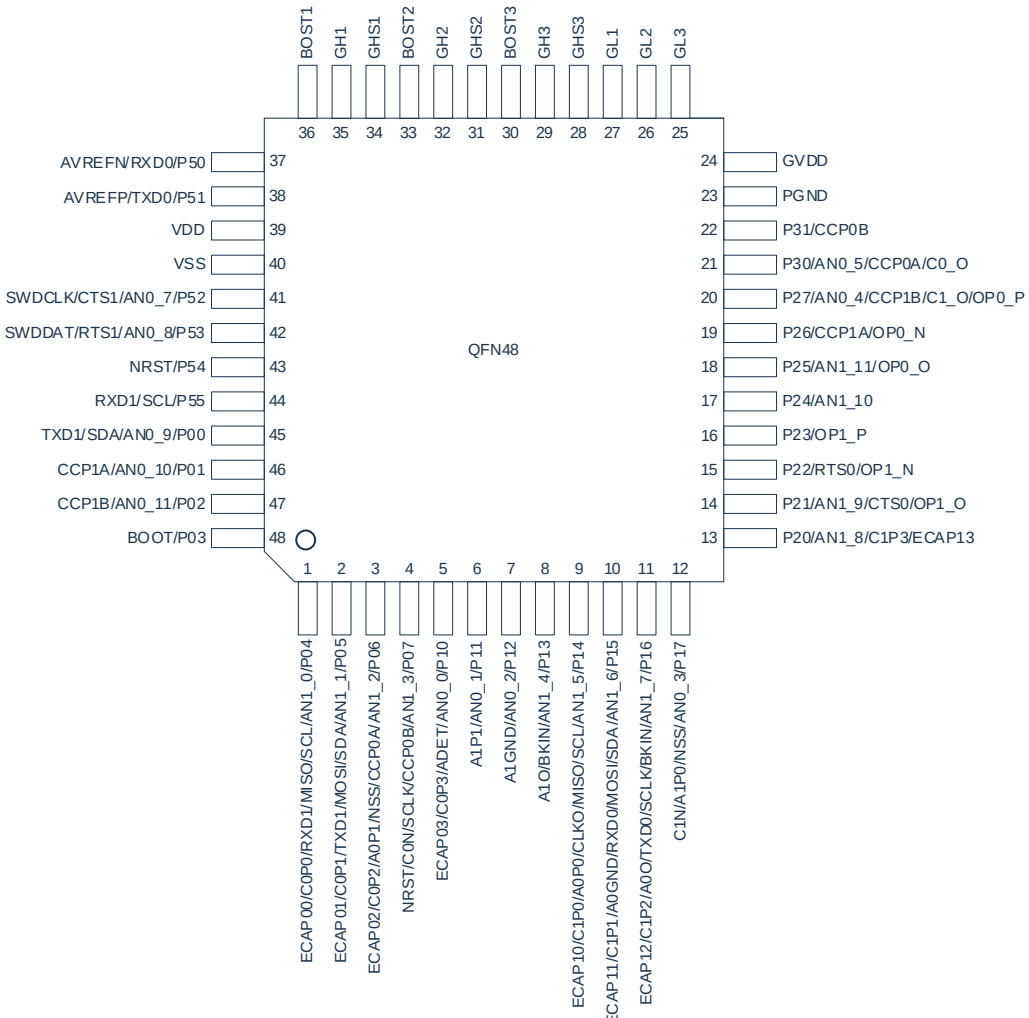
3. Pin definition

3.1 Pin description

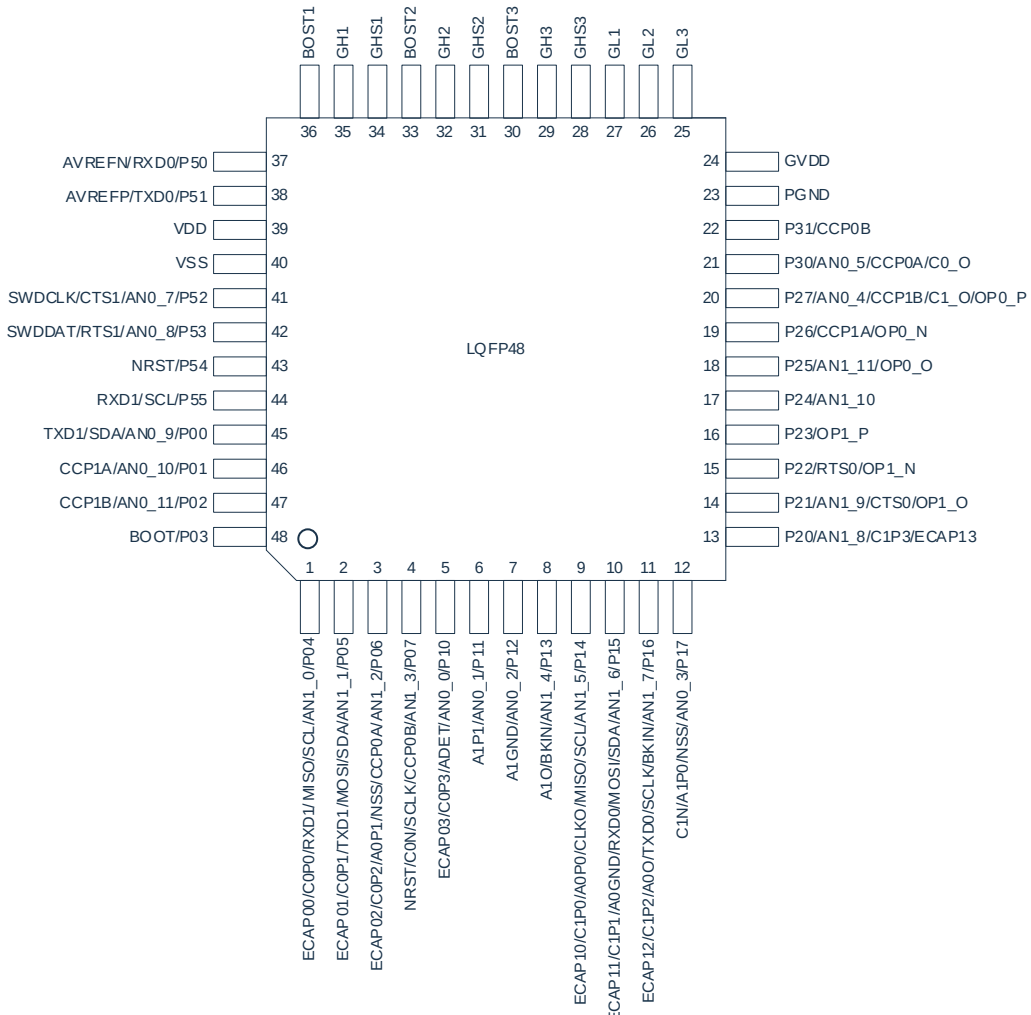
3.1.1 CMS32M5710 (LQFP48)



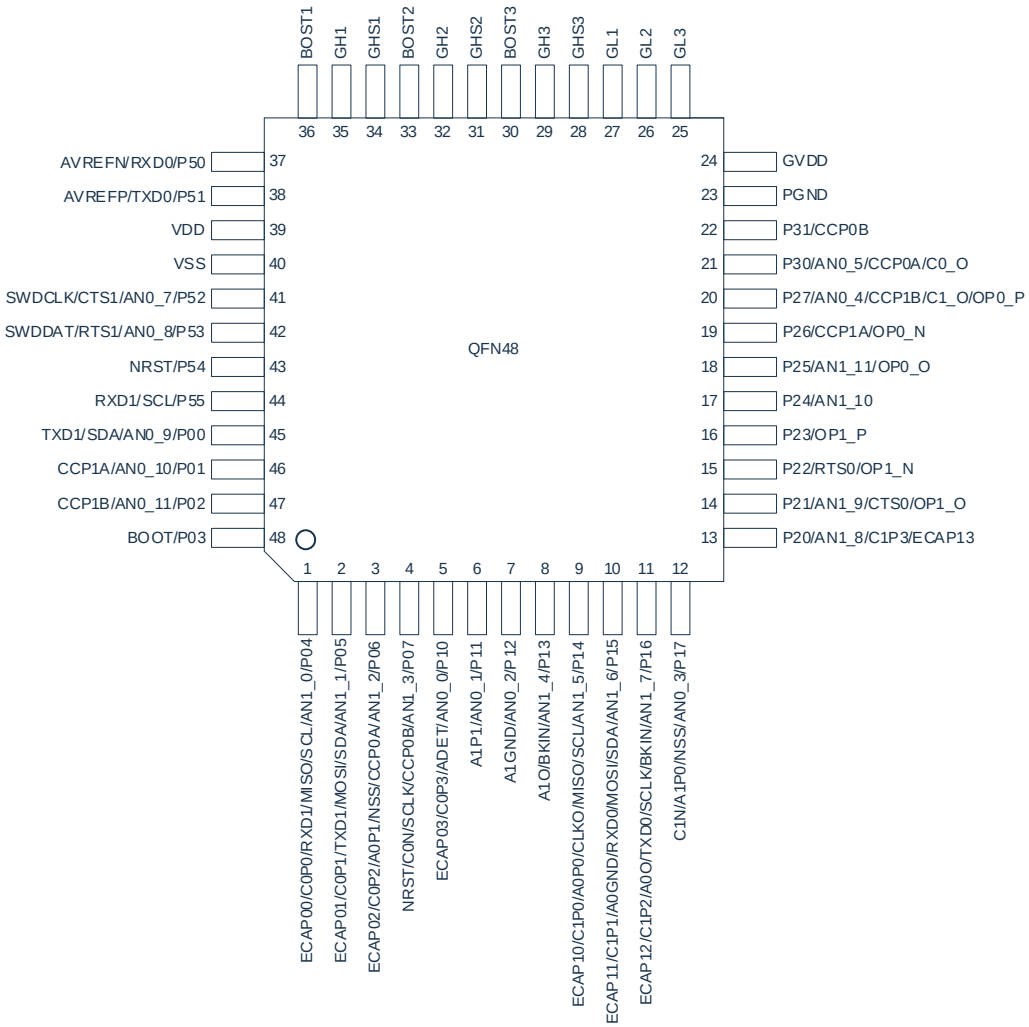
3.1.2 CMS32M5733 (QFN48)



3.1.3 CMS32M5736（LQFP48）



3.1.4 CMS32M5736 (QFN48)



3.2 Pin function description

The symbols in the table below are explained as follows：

Pin name	Symbol description
I/O	Digital input/output
I	Digital input
O	Digital output
AI	Analog input
AO	Analog output
P	Power source or ground

3.2.1 CMS32M5710 series

Pin number LQFP48	Pin name	Pin type	Description
1	P04	I/O	general purpose input/output pin
	AN1_0	AI	ADCB analog input channel 0
	C0P0	AI	ACMP0 positive input channel 0
	SCL	I/O	I2C clock input/output pin
	MISO	I/O	SPI Master input/slave output pin
	RXD1	I	UART1 data input pin
	ECAP00	I	ACMP0 positive input channel 0 capture input
2	P05	I/O	general purpose input/output pin
	AN1_1	AI	ADCB analog input channel 1
	C0P1	AI	ACMP0 positive input channel 1
	SDA	I/O	I2C data input/output pin
	MOSI	I/O	SPI master output/slave input pin
	TXD1	O	UART1 data output pin
	ECAP01	I	ACMP0 positive input channel1 capture input
3	P06	I/O	general purpose input/output pin
	AN1_2	AI	ADCB analog input channel 2
	C0P2	AI	ACMP0 positive input channel 2
	A0P1	AI	PGA0 positive input channel 1
	CCP0A	I/O	CCP0 capture input/PWM output A pin
	NSS	I/O	SPI chip select pin
	ECAP02	I	ACMP0 positive input channel 2 capture input
4	P07	I/O	general purpose input/output pin
	AN1_3	AI	ADCB analog input channel 3
	C0N	AI	ACMP0 negative input channel
	CCP0B	I/O	CCP0 capture input/PWM output B pin
	SCLK	I/O	SPI clock input/output pin
	NRST	I	external reset pin
5	P10	I/O	general purpose input/output pin
	AN0_0	AI	ADC0 analog input channel 0
	C0P3	AI	ACMP0 positive input channel 3
	ADET	I	ADC external start digital input
	ECAP03	I	ACMP0 positive input channel 3 capture input

Pin number LQFP48	Pin name	Pin type	Description
6	P11	I/O	general purpose input/output pin
	AN0_1	AI	ADC0 analog input channel 1
	A1P1	AI	PGA1 positive input channel 1
7	P12	I/O	general purpose input/output pin
	AN0_2	AI	ADC0 analog input channel2
	A1GND	AI	PGA1 feedback ground input
8	P13	I/O	general purpose input/output pin
	AN1_4	AI	ADCB analog input channel 4
	A1O	AO	PGA1 output pin
	BKIN	I	EPWM brake input pin
9	P14	I/O	general purpose input/output pin
	AN1_5	AI	ADCB analog input channel 5
	C1P0	AI	ACMP1 positive input channel 0
	A0P0	AI	PGA0 positive input channel 0
	SCL	I/O	I2C clock input/output pin
	MISO	I/O	SPI Master input/slave output pin
	CLKO	O	System clock output pin
	ECAP10	I	ACMP1 positive input channel 0 capture input
10	P15	I/O	general purpose input/output pin
	AN1_6	AI	ADCB analog input channel 6
	C1P1	AI	ACMP1 positive input channel 1
	A0GND	AI	PGA0 feedback ground input
	SDA	I/O	I2C data input/output pin
	MOSI	I/O	SPI master output/slave input pin
	RXD0	I	UART0 data input pin
	ECAP11	I	ACMP1 positive input channel1 capture input
11	P16	I/O	general purpose input/output pin
	AN1_7	AI	ADCB analog input channel7
	C1P2	AI	ACMP1positive input channel2
	A0O	AO	PGA0 output pin
	SCLK	I/O	SPIclock input/output pin
	TXD0	O	UART0 data output pin
	BKIN	I	EPWM brake input
	ECAP12	I	ACMP1 positive input channel 2 capture input
12	P17	I/O	general purpose input/output pin
	AN0_3	AI	ADC0analoginput channel3
	C1N	AI	ACMP1negativeinput channel
	A1P0	AI	PGA1positive input channel0
	NSS	I/O	SPI chip select pin
13	P20	I/O	general purpose input/output pin
	AN1_8	AI	ADCB analog input channel 8
	C1P3	AI	ACMP1positive input channel3
	ECAP13	I	ACMP1 positive input channel3 capture input
14	P21	I/O	general purpose input/output pin
	AN1_9	AI	ADCB analog input channel 9
	OP1_O	AO	OP1 output pin

Pin number LQFP48	Pin name	Pin type	Description
	CTS0	I	UART0 allow transmit pin
15	P22	I/O	general purpose input/output pin
	OP1_N	AI	OP1 negative input channel
	RTS0	O	UART0 request send pin
16	P23	I/O	general purpose input/output pin
	OP1_P	AI	OP1 positive input channel
17	P24	I/O	general purpose input/output pin
	AN1_10	AI	ADCB analog input channel 10
18	P25	I/O	general purpose input/output pin
	AN1_11	AI	ADCB analog input channel 11
	OP0_O	AO	OP0 output pin
19	P26	I/O	general purpose input/output pin
	OP0_N	AI	OP0 negative input channel
	CCP1A	I/O	CCP1 capture input/PWM output A pin
20	P27	I/O	general purpose input/output pin
	AN0_4	AI	ADC0 analog input channel 4
	OP0_P	AI	OP0 positive input channel
	CCP1B	I/O	CCP1 capture input/PWM output B pin
	C1_O	O	ACMP1 digital output pin
21	P30	I/O	general purpose input/output pin
	AN0_5	AI	ADC0 analog input channel 5
	CCP0A	I/O	CCP0 capture input/PWM output A pin
	C0_O	O	ACMP0 digital output pin
22	P31	I/O	general purpose input/output pin
	CCP0B	I/O	CCP0 capture input/PWM output B pin
23	P32	I/O	general purpose input/output pin
	CTS1	I	UART1 allow transmit pin
24	P33	I/O	general purpose input/output pin
	RTS1	O	UART1 request send pin
25	P34	I/O	general purpose input/output pin
26	P35	I/O	general purpose input/output pin
27	P36	I/O	general purpose input/output pin
28	P37	I/O	general purpose input/output pin
	CTS0	I	UART0 allow transmit pin
29	P40	I/O	general purpose input/output pin
	AN0_6	AI	ADC0 analog input channel 6
	RTS0	O	UART0 request send pin
	BKIN	I	EPWM brake input pin
	BOOT	I	BOOT configure input pin
30	P41	I/O	general purpose input/output pin
	BKIN	I	EPWM brake input pin
31	P42	I/O	general purpose input/output pin
	EPWM5	O	EPWM output pin 5
32	P43	I/O	general purpose input/output pin
	EPWM4	O	EPWM output pin 4
33	P44	I/O	general purpose input/output pin

Pin number LQFP48	Pin name	Pin type	Description
	EPWM3	O	EPWM output pin 3
34	P45	I/O	general purpose input/output pin
	EPWM2	O	EPWM output pin 2
35	P46	I/O	general purpose input/output pin
	EPWM1	O	EPWM output pin 1
36	P47	I/O	general purpose input/output pin
	EPWM0	O	EPWM output pin 0
37	P50	I/O	general purpose input/output pin
	RXD0	I	UART0 data input pin
	AVREFN	AI	ADCB external reference negative
38	P51	I/O	general purpose input/output pin
	TXD0	O	UART0 data output pin
	AVREFP	AI	ADCB external reference positive
39	VDD	P	Power source
40	VSS	P	Ground
41	P52	I/O	general purpose input/output pin
	AN0_7	AI	ADC0 analog input channel 7
	CTS1	I	UART1 allow transmit pin
	SWDCLK	I	SWD simulation clock input pin
42	P53	I/O	general purpose input/output pin
	AN0_8	AI	ADC0 analog input channel 8
	RTS1	O	UART1 request send pin
	SWDDAT	I/O	SWD simulation data input/output pin
43	P54	I/O	general purpose input/output pin
	NRST	I	external reset pin
44	P55	I/O	general purpose input/output pin
	SCL	I/O	I2C clock input/output pin
	RXD1	I	UART1 data input pin
45	P00	I/O	general purpose input/output pin
	AN0_9	AI	ADC0 analog input channel 9
	SDA	I/O	I2C data input/output pin
	TXD1	O	UART1 data output pin
46	P01	I/O	general purpose input/output pin
	AN0_10	AI	ADC0 analog input channel 10
	CCP1A	I/O	CCP1 capture input/PWM output A pin
47	P02	I/O	general purpose input/output pin
	AN0_11	AI	ADC0 analog input channel 11
	CCP1B	I/O	CCP1 capture input/PWM output B pin
48	P03	I/O	general purpose input/output pin
	BOOT	I	BOOT configure input pin

3.2.2 CMS32M5736 series

Pin number LQFP48	Pin name	Pin type	Description
1	P04	I/O	general purpose input/output pin
	AN1_0	AI	ADCB analog input channel 0
	C0P0	AI	ACMP0 positive input channel 0
	SCL	I/O	I2C clock input/output pin
	MISO	I/O	SPI Master input/slave output pin
	RXD1	I	UART1 data input pin
	ECAP00	I	ACMP0 positive input channel 0 capture input
2	P05	I/O	general purpose input/output pin
	AN1_1	AI	ADCB analog input channel 1
	C0P1	AI	ACMP0 positive input channel 1
	SDA	I/O	I2C data input/output pin
	MOSI	I/O	SPI master output/slave input pin
	TXD1	O	UART1 data output pin
	ECAP01	I	ACMP0 positive input channel1 capture input
3	P06	I/O	general purpose input/output pin
	AN1_2	AI	ADCB analog input channel 2
	C0P2	AI	ACMP0 positive input channel 2
	A0P1	AI	PGA0 positive input channel 1
	CCP0A	I/O	CCP0 capture input/PWM output A pin
	NSS	I/O	SPI chip select pin
	ECAP02	I	ACMP0 positive input channel 2 capture input
4	P07	I/O	general purpose input/output pin
	AN1_3	AI	ADCB analog input channel 3
	C0N	AI	ACMP0 negative input channel
	CCP0B	I/O	CCP0 capture input/PWM output B pin
	SCLK	I/O	SPI clock input/output pin
	NRST	I	external reset pin
5	P10	I/O	general purpose input/output pin
	AN0_0	AI	ADC0 analog input channel 0
	C0P3	AI	ACMP0 positive input channel 3
	ADET	I	ADC external start digital input
	ECAP03	I	ACMP0 positive input channel 3 capture input
6	P11	I/O	general purpose input/output pin
	AN0_1	AI	ADC0 analog input channel 1
	A1P1	AI	PGA1 positive input channel 1
7	P12	I/O	general purpose input/output pin
	AN0_2	AI	ADC0 analog input channel2
	A1GND	AI	PGA1 feedback ground input
8	P13	I/O	general purpose input/output pin
	AN1_4	AI	ADCB analog input channel 4
	A1O	AO	PGA1 output pin
	BKIN	I	EPWM brake input pin
9	P14	I/O	general purpose input/output pin
	AN1_5	AI	ADCB analog input channel 5

Pin number LQFP48	Pin name	Pin type	Description
	C1P0	AI	ACMP1 positive input channel 0
	A0P0	AI	PGA0 positive input channel 0
	SCL	I/O	I2C clock input/output pin
	MISO	I/O	SPI Master input/slave output pin
	CLKO	O	System clock output pin
	ECAP10	I	ACMP1 positive input channel 0 capture input
10	P15	I/O	general purpose input/output pin
	AN1_6	AI	ADCB analog input channel 6
	C1P1	AI	ACMP1 positive input channel 1
	A0GND	AI	PGA0 feedback ground input
	SDA	I/O	I2C data input/output pin
	MOSI	I/O	SPI master output/slave input pin
	RXD0	I	UART0 data input pin
	ECAP11	I	ACMP1 positive input channel1 capture input
11	P16	I/O	general purpose input/output pin
	AN1_7	AI	ADCB analog input channel7
	C1P2	AI	ACMP1positive input channel2
	A0O	AO	PGA0 output pin
	SCLK	I/O	SPIclock input/output pin
	TXD0	O	UART0 data output pin
	BKIN	I	EPWM brake input
	ECAP12	I	ACMP1 positive input channel 2 capture input
12	P17	I/O	general purpose input/output pin
	AN0_3	AI	ADC0analoginput channel3
	C1N	AI	ACMP1negativeinput channel
	A1P0	AI	PGA1positive input channel0
	NSS	I/O	SPI chip select pin
13	P20	I/O	general purpose input/output pin
	AN1_8	AI	ADCB analog input channel 8
	C1P3	AI	ACMP1positive input channel3
	ECAP13	I	ACMP1 positive input channel3 capture input
14	P21	I/O	general purpose input/output pin
	AN1_9	AI	ADCB analog input channel 9
	OP1_O	AO	OP1 output pin
	CTS0	I	UART0 allow transmit pin
15	P22	I/O	general purpose input/output pin
	OP1_N	AI	OP1 negative input channel
	RTS0	O	UART0 request send pin
16	P23	I/O	general purpose input/output pin
	OP1_P	AI	OP1 positive input channel
17	P24	I/O	general purpose input/output pin
	AN1_10	AI	ADCB analog input channel 10
18	P25	I/O	general purpose input/output pin
	AN1_11	AI	ADCB analog input channel 11
	OP0_O	AO	OP0 output pin
19	P26	I/O	general purpose input/output pin

Pin number LQFP48	Pin name	Pin type	Description
	OP0_N	AI	OP0 negative input channel
	CCP1A	I/O	CCP1 capture input/PWM output A pin
20	P27	I/O	general purpose input/output pin
	AN0_4	AI	ADC0 analog input channel 4
	OP0_P	AI	OP0 positive input channel
	CCP1B	I/O	CCP1 capture input/PWM output B pin
	C1_O	O	ACMP1 digital output pin
21	P30	I/O	general purpose input/output pin
	AN0_5	AI	ADC0 analog input channel 5
	CCP0A	I/O	CCP0 capture input/PWM output A pin
	C0_O	O	ACMP0 digital output pin
22	P31	I/O	general purpose input/output pin
	CCP0B	I/O	CCP0 capture input/PWM output B pin
37	P50	I/O	general purpose input/output pin
	RXD0	I	UART0 data input pin
	AVREFN	AI	ADCB external reference negative
38	P51	I/O	general purpose input/output pin
	TXD0	O	UART0 data output pin
	AVREFP	AI	ADCB external reference positive
39	VDD	P	Power source
40	VSS	P	Ground
41	P52	I/O	general purpose input/output pin
	AN0_7	AI	ADC0 analog input channel 7
	CTS1	I	UART1 allow transmit pin
	SWDCLK	I	SWD simulation clock input pin
42	P53	I/O	general purpose input/output pin
	AN0_8	AI	ADC0 analog input channel 8
	RTS1	O	UART1 request send pin
	SWDDAT	I/O	SWD simulation data input/output pin
43	P54	I/O	general purpose input/output pin
	NRST	I	external reset pin
44	P55	I/O	general purpose input/output pin
	SCL	I/O	I2C clock input/output pin
	RXD1	I	UART1 data input pin
45	P00	I/O	general purpose input/output pin
	AN0_9	AI	ADC0 analog input channel 9
	SDA	I/O	I2C data input/output pin
	TXD1	O	UART1 data output pin
46	P01	I/O	general purpose input/output pin
	AN0_10	AI	ADC0 analog input channel 10
	CCP1A	I/O	CCP1 capture input/PWM output A pin
47	P02	I/O	general purpose input/output pin
	AN0_11	AI	ADC0 analog input channel 11
	CCP1B	I/O	CCP1 capture input/PWM output B pin
48	P03	I/O	general purpose input/output pin
	BOOT	I	BOOT configure input pin

Pin number LQFP48	Pin name	Pin type	Description
23	PGND	P	Built-in pre-drive ground pin
24	GVDD	P	Built-in pre-drive power pin
25	GL3	O	Phase 3 low-side gate driveoutput pin
26	GL2	O	Phase 2 low-side gate drive output pin
27	GL1	O	Phase 1 low-side gate drive output pin
28	GHS3	P	Phase 3 high-side floating pin
29	GH3	O	Phase 3 high-side gate drive output pin
30	BOST3	P	Phase 3 high-side bootstrap power supply pin
31	GHS2	P	Phase 2 high-side floating pin
32	GH2	O	Phase 2 high-side gate drive output pin
33	BOST2	P	Phase 2 high-side bootstrap power supply pin
34	GHS1	P	Phase 1 high-side floating pin
35	GH1	O	Phase 1 high-side gate drive output pin
36	BOST1	P	Phase 1 high-side bootstrap power supply pin

3.2.3 CMS32M5733/CMS32M5736 series

Pin number	Pin name	Pin type	Description
QFN48			
1	P04	I/O	general purpose input/output pin
	AN1_0	AI	ADCB analog input channel 0
	C0P0	AI	ACMP0 positive input channel0
	SCL	I/O	I2C clock input/output pin
	MISO	I/O	SPI master input/slave output pin
	RXD1	I	UART1 data input pin
	ECAP00	I	ACMP0 positive input channel0 capture input
2	P05	I/O	general purpose input/output pin
	AN1_1	AI	ADCB analog input channel 1
	C0P1	AI	ACMP0 positive input channel1
	SDA	I/O	I2C data input/output pin
	MOSI	I/O	SPI master output/slave input pin
	TXD1	O	UART1 data output pin
	ECAP01	I	ACMP0 positive input channel1 capture input
3	P06	I/O	general purpose input/output pin
	AN1_2	AI	ADCB analog input channel 2
	C0P2	AI	ACMP0 positive input channel2
	A0P1	AI	PGA0 positive input channel1
	CCP0A	I/O	CCP0 capture input/PWM output A pin
	NSS	I/O	SPI chip select pin
	ECAP02	I	ACMP0 positive input channel2 capture input
4	P07	I/O	general purpose input/output pin
	AN1_3	AI	ADCB analog input channel 3
	C0N	AI	ACMP0 negative input channel
	CCP0B	I/O	CCP0 capture input/PWM output B pin
	SCLK	I/O	SPI clock input/output pin
	NRST	I	external reset pin
5	P10	I/O	general purpose input/output pin
	AN0_0	AI	ADC0 analog input channel 0
	C0P3	AI	ACMP0 positive input channel3
	ADET	I	ADC external start digital input
	ECAP03	I	ACMP0 positive input channel3 capture input
6	P11	I/O	general purpose input/output pin
	AN0_1	AI	ADC0 analog input channel 1
	A1P1	AI	PGA1 positive input channel1
7	P12	I/O	general purpose input/output pin
	AN0_2	AI	ADC0 analog input channel 2
	A1GND	AI	PGA1 feedback ground input
8	P13	I/O	general purpose input/output pin
	AN1_4	AI	ADCB analog input channel 4
	A1O	AO	PGA1 output pin
	BKIN	I	EPWM brake input pin
9	P14	I/O	general purpose input/output pin
	AN1_5	AI	ADCB analog input channel 5

Pin number QFN48	Pin name	Pin type	Description
	C1P0	AI	ACMP1 positive input channel0
	A0P0	AI	PGA0 positive input channel0
	SCL	I/O	I2C clock input/output pin
	MISO	I/O	SPI master input/slave output pin
	CLKO	O	System clock output pin
	ECAP10	I	ACMP1 positive input channel0 capture input
10	P15	I/O	general purpose input/output pin
	AN1_6	AI	ADCB analog input channel 6
	C1P1	AI	ACMP1 positive input channel1
	A0GND	AI	PGA0 feedback ground input
	SDA	I/O	I2C data input/output pin
	MOSI	I/O	SPI master output/slave input pin
	RXD0	I	UART0 data input pin
	ECAP11	I	ACMP1 positive input channel1 capture input
11	P16	I/O	general purpose input/output pin
	AN1_7	AI	ADCB analog input channel 7
	C1P2	AI	ACMP1 positive input channel2
	A0O	AO	PGA0 output pin
	SCLK	I/O	SPI clock input/output pin
	TXD0	O	UART0 data output pin
	BKIN	I	EPWM brake input
	ECAP12	I	ACMP1 positive input channel2 capture input
12	P17	I/O	general purpose input/output pin
	AN0_3	AI	ADC0 analog input channel 3
	C1N	AI	ACMP1 negative input channel
	A1P0	AI	PGA1 positive input channel0
	NSS	I/O	SPI chip select pin
13	P20	I/O	general purpose input/output pin
	AN1_8	AI	ADCB analog input channel 8
	C1P3	AI	ACMP1 positive input channel3
	ECAP13	I	ACMP1 positive input channel3 capture input
14	P21	I/O	general purpose input/output pin
	AN1_9	AI	ADCB analog input channel 9
	OP1_O	AO	OP1 output pin
	CTS0	I	UART0 allow transmit pin
15	P22	I/O	general purpose input/output pin
	OP1_N	AI	OP1 negative input channel
	RTS0	O	UART0 request send pin
16	P23	I/O	general purpose input/output pin
	OP1_P	AI	OP1 positive input channel
17	P24	I/O	general purpose input/output pin
	AN1_10	AI	ADCB analog input channel 10
18	P25	I/O	general purpose input/output pin
	AN1_11	AI	ADCB analog input channel 11
	OP0_O	AO	OP0 output pin
19	P26	I/O	general purpose input/output pin

Pin number QFN48	Pin name	Pin type	Description
	OP0_N	AI	OP0 negative input channel
	CCP1A	I/O	CCP1 capture input/PWM output A pin
20	P27	I/O	general purpose input/output pin
	AN0_4	AI	ADC0 analog input channel 4
	OP0_P	AI	OP0 positive input channel
	CCP1B	I/O	CCP1 capture input/PWM output B pin
	C1_O	O	ACMP1 digital output pin
21	P30	I/O	general purpose input/output pin
	AN0_5	AI	ADC0 analog input channel 5
	CCP0A	I/O	CCP0 capture input/PWM output A pin
	C0_O	O	ACMP0 digital output pin
22	P31	I/O	general purpose input/output pin
	CCP0B	I/O	CCP0 capture input/PWM output B pin
-	P32	I/O	general purpose input/output pin
	CTS1	I	UART1 allow transmit pin
-	P33	I/O	general purpose input/output pin
	RTS1	O	UART1 request send pin
-	P34	I/O	general purpose input/output pin
-	P35	I/O	general purpose input/output pin
-	P36	I/O	general purpose input/output pin
-	P37	I/O	general purpose input/output pin
	CTS0	I	UART0 allow transmit pin
-	P40	I/O	general purpose input/output pin
	AN0_6	AI	ADC0 analog input channel 6
	RTS0	O	UART0 request send pin
	BKIN	I	EPWM brake input pin
	BOOT	I	BOOT configure input pin
-	P41	I/O	general purpose input/output pin
	BKIN	I	EPWM brake input pin
-	P42	I/O	general purpose input/output pin
	EPWM5	O	EPWM output pin 5
-	P43	I/O	general purpose input/output pin
	EPWM4	O	EPWM output pin 4
-	P44	I/O	general purpose input/output pin
	EPWM3	O	EPWM output pin 3
-	P45	I/O	general purpose input/output pin
	EPWM2	O	EPWM output pin 2
-	P46	I/O	general purpose input/output pin
	EPWM1	O	EPWM output pin 1
-	P47	I/O	general purpose input/output pin
	EPWM0	O	EPWM output pin 0
37	P50	I/O	general purpose input/output pin
	RXD0	I	UART0 data input pin
	AVREFN	AI	ADCB external reference negative
38	P51	I/O	general purpose input/output pin
	TXD0	O	UART0 data output pin

Pin number QFN48	Pin name	Pin type	Description
	AVREFP	AI	ADCB external reference positive
39	VDD	P	Power source
40	VSS	P	ground
41	P52	I/O	general purpose input/output pin
	AN0_7	AI	ADC0 analog input channel7
	CTS1	I	UART1 allow transmit pin
	SWDCLK	I	SWD simulation clock input pin
42	P53	I/O	general purpose input/output pin
	AN0_8	AI	ADC0 analog input channel 8
	RTS1	O	UART1 request send pin
	SWDDAT	I/O	SWD simulation data input/output pin
43	P54	I/O	general purpose input/output pin
	NRST	I	external reset pin
44	P55	I/O	general purpose input/output pin
	SCL	I/O	I2C clock input/output pin
	RXD1	I	UART1 data input pin
45	P00	I/O	general purpose input/output pin
	AN0_9	AI	ADC0 analog input channel 9
	SDA	I/O	I2C data input/output pin
	TXD1	O	UART1 data output pin
46	P01	I/O	general purpose input/output pin
	AN0_10	AI	ADC0 analog input channel10
	CCP1A	I/O	CCP1 capture input/PWM output A pin
47	P02	I/O	general purpose input/output pin
	AN0_11	AI	ADC0 analog input channel 11
	CCP1B	I/O	CCP1 capture input/PWM output B pin
48	P03	I/O	general purpose input/output pin
	BOOT	I	BOOT configure input pin
23	PGND	P	Built-in pre-drive ground pin
24	GVDD	P	Built-in pre-drive power pin
25	GL3	O	Phase 3 low-side gate driveoutput pin
26	GL2	O	Phase 2 low-side gate drive output pin
27	GL1	O	Phase 1 low-side gate drive output pin
28	GHS3	P	Phase 3 high-side floating pin
29	GH3	O	Phase 3 high-side gate drive output pin
30	BOST3	P	Phase 3 high-side bootstrap power supply pin
31	GHS2	P	Phase 2 high-side floating pin
32	GH2	O	Phase 2 high-side gate drive output pin
33	BOST2	P	Phase 2 high-side bootstrap power supply pin
34	GHS1	P	Phase 1 high-side floating pin
35	GH1	O	Phase 1 high-side gate drive output pin
36	BOST1	P	Phase 1 high-side bootstrap power supply pin

3.3 GPIO feature

The pins share multiple functions, and each I/O port can be configured as a corresponding digital function or analog function. I/O as a general-purpose GPIO port has the following characteristics:

- It can be configured as normal input, pull-up input, pull-down input, push-pull output, and open-drain output mode without pull-up.
- It can be configured to high level, low level, rising edge, falling edge, double edge trigger interrupt.
- It can be configured to high level, low level, rising edge, falling edge to wake up the chip sleep/deep sleep/stop mode.
- Configurable 2 levels of I/O speed.
- Configurable 2 levels of output current.

3.4 Pin function list

Port multiplexing function allocation list：

Function symbol									
	CONFIG	0	1	2	3	4	5	6	7
P00		GPIO	ANA	TXD1	SDA				
P01		GPIO	ANA				CCP1A		
P02		GPIO	ANA				CCP1B		
P03	BOOT	GPIO							
P04		GPIO/ECAP00	ANA	RXD1	SCL	MISO			
P05		GPIO/ECAP01	ANA	TXD1	SDA	MOSI			
P06		GPIO/ECAP02	ANA			NSS	CCP0A		
P07	NRST	GPIO	ANA			SCLK	CCP0B		
P10		GPIO/ECAP03	ANA						ADET
P11		GPIO	ANA						
P12		GPIO	ANA						
P13		GPIO	ANA					BKIN	
P14		GPIO/ECAP10	ANA		SCL	MISO			CLKO
P15		GPIO/ECAP11	ANA	RXD0	SDA	MOSI			
P16		GPIO/ECAP12	ANA	TXD0		SCLK		BKIN	
P17		GPIO	ANA			NSS			
P20		GPIO/ECAP13	ANA						
P21		GPIO	ANA	CTS0					
P22		GPIO	ANA	RTS0					
P23		GPIO	ANA						
P24		GPIO	ANA						
P25		GPIO	ANA						
P26		GPIO	ANA				CCP1A		
P27		GPIO	ANA				CCP1B		C1_O
P30		GPIO	ANA				CCP0A		C0_O
P31		GPIO					CCP0B		
P32		GPIO		CTS1					
P33		GPIO		RTS1					
P34		GPIO							
P35		GPIO							
P36		GPIO							
P37		GPIO		CTS0					
P40	BOOT	GPIO	ANA	RTS0				BKIN	
P41		GPIO						BKIN	
P42		GPIO						EPWM5	
P43		GPIO						EPWM4	
P44		GPIO						EPWM3	
P45		GPIO						EPWM2	
P46		GPIO						EPWM1	
P47		GPIO						EPWM0	
P50		GPIO	ANA	RXD0					
P51		GPIO	ANA	TXD0					
P52		GPIO	ANA	CTS1					SWDCLK
P53		GPIO	ANA	RTS1					SWDDAT
P54	NRST	GPIO							
P55		GPIO		RXD1	SCL				

Analog function list：

	ANA (can use multiple analog feature at the same time)				
	ADC0	ADCB	ACMP	PGA	OP
P00	AN0_9				
P01	AN0_10				
P02	AN0_11				
P03					
P04		AN1_0	C0P0		
P05		AN1_1	C0P1		
P06		AN1_2	C0P2	A0P1	
P07		AN1_3	C0N		
P10	AN0_0		C0P3		
P11	AN0_1			A1P1	
P12	AN0_2			A1GND	
P13		AN1_4		A1O	
P14		AN1_5	C1P0	A0P0	
P15		AN1_6	C1P1	A0GND	
P16		AN1_7	C1P2	A0O	
P17	AN0_3		C1N	A1P0	
P20		AN1_8	C1P3		
P21		AN1_9			OP1_O
P22					OP1_N
P23					OP1_P
P24		AN1_10			
P25		AN1_11			OP0_O
P26					OP0_N
P27	AN0_4				OP0_P
P30	AN0_5				
P31					
P32					
P33					
P34					
P35					
P36					
P37					
P40	AN0_6				
P41					
P42					
P43					
P44					
P45					
P46					
P47					
P50		AVREFN			
P51		AVREFP			
P52	AN0_7				
P53	AN0_8				
P54					
P55					

Note：

(1) When configured as 0, it is a GPIO function, and its input Schmitt is normally open (including when the state is output).

When configured as 1, all GPIO functions are closed, including the output circuit, Schmitt input circuit, and both up

and down are closed.

(2) When configured as a digital function, the analog function can also be used. For example, when P04 is configured as a GPIO to use the ECAP function, the comparator C0P0 function can be used at the same time.

(3) The port supports the simultaneous use of multiple analog functions, such as the P25 can use the op amp function and the AD channel function at the same time.

(4) When only using the analog function, it is recommended to set the configuration to 1 and turn off the digital circuit to reduce power consumption.

Configuration priority of function multi-port mapping:

(1) Input function:

If there are two or more ports configured with the same input function at the same time, configure the selection according to the priority order of P00, P01,..., P55 from high to low. If P13 and P16 are configured as BKIN ports at the same time, P13 has a high priority. P13 realizes the function of BKIN, while P16 is not configured as the function of BKIN.

(2) Output function:

The output function is not restricted by the priority order. If there are multiple ports configured with the same output function, the function will be output at these ports at the same time.

4. Function summary

4.1 ARM Cortex–M0 core

Cortex® -M0 processor is a configurable 32-bit RISC processor with multi-stage pipeline. It has an AMBA AHB-Lite interface and contains NVIC components, as well as optional hardware debugging functions. The processor can execute Thumb instructions and is compatible with other Cortex® -M series processors. The processor supports two working modes-Threadmode and Handlermode. The system enters Handlermode when abnormal, and the abnormal return can only be executed in Handlermode. Thread mode can be entered after system reset and abnormal return.

4.2 Memory

4.2.1 Program memory (FLASH)

The program memory is divided into two areas: APROM and BOOT, you can choose to boot from APROM or BOOT area when power is on.

Different product models have different program space sizes, depending on the specific model, the maximum space is 64KB.

The maximum space of BOOT is 4KB.

This series of products can be configured with the size of BOOT, the configuration method is as follows:

64K (Program storage area)				
Address space allocation method	APROM area		BOOT area	
Method 0	64KB	0000H-FFFFH	--	--
Method 1	63KB	0000H-FBFFH	1KB	FC00H-FFFFH
Method 2	62KB	0000H-F7FFH	2KB	F800H-FFFFH
Method 3	60KB	0000H-EFFFH	4KB	F000H-FFFFH

4.2.2 Non-volatile data storage (Data FLASH)

Data FLASH has a space size of 1KB and is divided into two sectors. Can store the data that users need to save when power off.

4.2.3 Data storage (SRAM)

The maximum data memory is 8KB. Except 2KB at the beginning of the initial address, write protection can be set for every 2KB later.

4.3 Interrupt control

Cortex®-M0 CPU provides a Nested Vectored Interrupt Controller (NVIC) for interrupt processing, with the following features:

- Support nested vector interrupt.
- Automatically save and restore processor state.
- Dynamically change priority.
- Simplified and defined interruption time.

The system provides multiple peripheral interrupt sources, including GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, CCP, WWDT, EPWM, ADC0, ADCB, ACMP, UART0, UART1, TIMER0, TIMER1, TIMER2, TIMER3, WDT, I2C, SPI, SYS_CHK, the actual number of interrupt sources varies from product to product. Each interrupt supports 4 levels of interrupt priority, the highest priority is 0, the lowest priority is 3, and the default priority is 0.

4.4 Clock control

The clock controller provides the clock source for the entire chip, including the system clock and all peripheral equipment clocks. The controller selects the clock through a separate clock switch, clock source selection and frequency divider, and can also output clock through the IO port.

The clock source can be selected from the following two types:

- Internal high-speed oscillator HSI (48MHz/64MHz) .
- Internal low-speed oscillator LSI (40KHz) .

Clock output can choose the following two types:

- AHB bus clock AHBCLK.
- Internal high-speed oscillator HIS.

4.5 Power management

4.5.1 Operating mode

The system has 4 different working modes to meet the power consumption requirements of different applications.

- Normal mode：MCU is in normal working mode, peripherals are running normally, LDO is turned on.
- Sleep mode：MCU is in sleep mode, CPU stops working, peripherals are running normally, LDO is turned on.
- Deep sleep mode：MCU is in deep sleep mode, CPU stops working, peripherals only work with WDT, and LDO is turned on.
- Stop mode：MCU is in stop mode, CPU stops working, peripherals stop working, LDO is in low power mode.

4.5.2 Low voltage reset (LVR)

This series of products contains a low-voltage reset circuit, when the power supply voltage is lower than the set detection voltage, the system is reset.

There are 3 choices for low voltage detection voltage: 1.9V/2.1V/2.6V.

4.5.3 Low voltage detection (LVD)

This series of products contains a low-voltage detection circuit that can compare the power supply voltage with the set detection voltage. If the power supply voltage is lower than the set detection voltage, an interrupt request signal is generated.

There are 8 options for detection voltage: 4.2V/4.0V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V.

4.6 Tmer

4.6.1 System timer (SysTick)

Cortex®-M0 has a built-in system timer SysTick. SysTick provides a simple 24-bit write clear, count down, and auto-load initial value functions. It also has a register with a flexible control mechanism. The counter can be used as a tick timer of a real-time operating system (RTOS) or as a simple timer peripheral

4.6.2 Watchdog timer (WDT)

The watchdog timer is a 32-bit down counter with 40KHz as the counting clock source. When the system runs to an unknown state, the watchdog can be used to reset the system, thus avoiding the system from entering an infinite loop. The watchdog timer has the following characteristics:

- Counting clock can choose 1, 16, 256 frequency division.
- Support watchdog reset system.
- Support watchdog timer interrupt.
- Support watchdog interrupt to wake up the system from sleep/deep sleep mode.

4.6.3 Window watchdog timer (WWDT)

The window watchdog timer is a 6-bit down counter. The window watchdog timer is used to perform a system reset within a specific window time to prevent the program from going to an uncontrollable state under unpredictable conditions. Window watchdog timer has the following characteristics:

- 6-bit window comparison value.
- Counting clock can choose 14 kinds of frequency division ratio.
- Supports interrupt generation when the window watchdog count value is equal to the window comparison value.
- Supports loading data when the window watchdog count value is greater than the window comparison value, generating a system reset.
- Support the system reset when the window count value is decremented to 0.

4.6.4 General timer (TIMER0/1/2/3)

This series of products includes 4 programmable 32-bit/16-bit down counters, which can provide users with convenient timing counting functions. TIMER0/TIMER1/ TIMER2/TIMER3 has the following characteristics:

- Counting clock can choose 1, 16, 256 frequency division.
- There are three counting operation modes: single trigger, periodic counting, and continuous counting.
- Support delay load counting initial value function.
- Supports generating an interrupt when the counter is decremented to 0.
- Support timer interrupt wake up sleep mode.

4.7 Enhanced digital peripherals

4.7.1 Cyclic redundancy check unit (CRC)

Cyclic Redundancy Check CRC is the most commonly used error check code in the field of data communication. Its characteristic is that the length of the information field and the check field can be arbitrarily selected. The chip CRC check unit generates polynomials using $X^{16}+X^{12}+X^5+1$" CRC16-CCITT), and the data to be checked is specified by the program, so that the module is not limited to the code flash area but can be used for multi-purpose checking.

4.7.2 Hardware divider (HWDIV)

This series of products includes a 32bit/32bit hardware divider, which has the following characteristics:

- Support unsigned or signed number division.
- Has divide by zero flag indicator bit.
- The bit width of the quotient and remainder are both 32 bits.
- Write the divisor register to start the division operation.
- 6 HCLK clocks to complete the operation.

4.7.3 Capture/Compare/Pulse Width Modulation Module (CCP0/1)

This series of products includes 2 groups of CCP modules (CCP0/CCP1), each group of CCP corresponds to A and B channels. CCP module supports PWM output, capture mode0, capture mode1, interrupt.

(1) PWM output has the following characteristics:

- The A and B channels of CCP0 share one period register, and the A and B channels of CCP1 share another period register.
- The duty cycle of CCP0/CCP1's A and B outputs can be set independently.
- Up to 4 PWM channels can be output.
- Choice of output polarity.

(2) Capture mode0 has the following characteristics:

- CCP0 can choose A or B as the external capture input signal.
- CCP1 can choose A or B as the external capture input signal.
- Software start counting and rising edge capture can be selected; software start counting and falling edge capture; rising edge counting and falling edge capture; falling edge counting and rising edge capture, total of 4 capture methods.
- The capture condition is triggered and the counter stops.

(3) Capture mode1 has the following characteristics:

- Only CCP1 has capture mode1.
- CAP0, CAP1, CAP2, CAP3, 4 capture channels, each capture channel has a 4-bit control to select different inputs.
- Software capture mode triggered by write register can be selected.
- The edge capture mode of the rising edge, falling edge and dual edge trigger of external signal can be selected.
- Support CCP1 capture trigger CCP0 counter load enable.

(4) CCP modele has the following interrupts:

- PWM interrupt.
- Capture mode0 interrupt.
- CAP0, CAP1, CAP2, CAP3 interrupt of capture mode 1.
- Counter overflow interrupt.

4.7.4 Enhanced PWM (EPWM)

The enhanced PWM module supports 6 PWM generators, and the period and duty cycle can be set independently. EPWM has the following characteristics:

- Support single and continuous 2 types of waveform output.
- Support 4 control modes: independent, complementary, synchronous, and group control.
- Counting clock can choose 1, 2, 4, 8, 16 frequency division.
- Support two counting modes: edge alignment and center alignment.
- Support 4 loading and update methods.
- Support dead zone programming.
- Choice of output polarity
- Support cycle, compare up, compare down, zero interrupt.
- Support fault brake protection and recovery function (soft/hardware trigger and software/hardware recovery).

4.8 Communication module

4.8.1 Universal Asynchronous Receiver Transmitter (UART0/1)

This series of products includes 2 full-duplex asynchronous communication interfaces, UART0 and UART1. The UART0/1 transceiver has the following characteristics:

- Full duplex, asynchronous communication.
- Register structure complies with 16550 industry standard.
- 16 bytes transmit FIFO and 16 bytes receive FIFO.
- Support hardware automatic flow control function (CTS, RTS).
- Support software flow control function (XOFF, XON)
- Choice of the receive buffer trigger level
- The data bit length can be set to 5~8 bits.
- Stop bit length can be set to 1, 1.5 or 2 bits.
- The generation and detection of parity, no check or fixed check bits can be set.

4.8.2 I^2C inter-integrated circuit controller (I^2C)

This series of products includes a two-wire bidirectional serial bus controller I^2C. The I^2C controller has the following characteristics:

- Standard I^2C compatible bus interface.
- Support master/slave mode, two-way data transfer between master and slave.
- Support simultaneous data arbitration between multiple hosts to avoid serial data damage on the bus.
- The bus adopts serial synchronous clock, which can realize transmission between devices at different rates.
- Programmable clock can be used for multiple rate control.
- Support 7-bit/10-bit slave address mode.
- Support multi-address recognition.

4.8.3 Serial Peripheral Interface Controller (SSP/SPI)

This series of products includes a synchronous serial controller SSP/SPI working in full-duplex mode. The SSP/SPI controller has the following characteristics:

- Compatible with Motorola's SPI, TI's 4-wire SSI and NS Microwire bus.
- Support host or slave mode.
- Configurable send bit length.
- Configurable clock polarity and phase.
- Clock rate programmable control.
- Provide 8 16-bit transmit/receive FIFO

4.9 Analog module

4.9.1 Low-speed analog-to-digital conversion (ADC0)

This series of products includes a 12-bit successive approximation analog-to-digital converter (ADC0), which supports single and continuous 2 conversion modes. ADC0 also has the following characteristics:

- Analog input voltage range: AVSS(VSS) ~ AVDD(VDD).
- Maximum sampling speed：100Ksps.
- Up to 20 single-ended analog input channels.
- The single conversion time is: 18.5*T_{ADCK}.
- Single mode: Perform an A/D conversion on the specified channel.
- Continuous mode: Perform A/D conversion on all selected channels.
- Support external input signal to trigger ADC conversion.
- Support interrupt generation after conversion.
- Built-in AD conversion result comparator.
- The conversion result of each channel is stored in the corresponding data register.
- Channels 12-19 can test dedicated analog voltage signals (output port of OP0/1, output port of PGA0/1, temperature sensor, internal reference, ADC reference positive/negative, etc.).

4.9.2 Fast analog-to-digital conversion (ADCB)

This series of products includes a 12-bit successive approximation analog-to-digital converter (ADCB), which supports single and continuous conversion modes. ADCB also has the following characteristics:

- Analog input voltage range: AVSS(VSS/AVREFN) ~ AVDD(VDD/AVREFP).
- Maximum sampling rate: 1.2Msps.
- Up to 20 single-ended analog input channels.
- Support two power consumption modes: high-speed mode and low-current mode.
- The single sampling and conversion time in high-speed mode is: 52*T_{ADCK}((sampling time is set to 13.5*T_{ADCK}).
- Single mode: Perform an A/D conversion on the specified channel.
- Continuous mode: Perform A/D conversion on all selected channels.
- Support external input signal to trigger ADC conversion.
- Support interrupt generation after conversion.
- Built-in AD conversion result comparator.
- The conversion result of each channel is stored in the corresponding data register.
- Channels 12-19 can test dedicated analog voltage signals (output port of OP0/1, output port of PGA0/1, temperature sensor, internal reference, ADC reference positive/negative, etc.).

4.9.3 Analog comparator (ACMP0/1)

This series of products contains 2 analog comparators, ACMP0 and ACMP1. ACMP0/1 has the following characteristics:

- Analog input voltage range: 0~(VDD-1.5V).
- Support single/double hysteresis voltage selection (10mV/20mV/60mV-typical value).
- Positive end can select multiple port input.
- negative end can select port input or internal reference voltage.
- A total of 16 gear selections for internal reference voltage division.
- Supports output filtering, a total of 11 levels of filtering time can be selected.
- Support output change to generate interrupt.

4.9.4 Operational Amplifier (OP0/1)

This series of products includes 2 basic operational amplifier modules OP0 and OP1, OP0/1 has the following characteristics:

- Can be configured as op amp mode and comparator mode.
- Output can be measured by ADC.

4.9.5 Programmable gain amplifier (PGA0/1)

This series of products includes 2 programmable gain amplifiers PGA0 and PGA1 modules, PGA0/1 has the following characteristics:

- Gain 8-level adjustable (4X/8X/10X/12X/14X/16X/32X).
- Output can be measured by ADC.

4.9.6 Temperature sensor (TS)

This series of products includes a temperature sensor, the temperature sensor has the following characteristics:

- Measurable temperature range: -40℃~105℃.
- Software modification possible.
- Output can be measured by ADC.

4.10 Memory control module

FLASH memory includes program memory (APROM/BOOT) and non-volatile data memory (Data FLASH), which can be accessed through related special function registers (SFR) to realize IAP function. FLASH memory supports the following operations:

- Byte read operation.
- Byte write operation.
- Byte erase operation.
- FLASH space CRC check operation.

4.11 Security relatives

4.11.1 Unique chip identification number (UID)

Each chip has a 96-bit unique identification number, which has been set at the factory and cannot be modified by the user, but it can be read through the memory module.

4.11.2 User's unique chip identification number (USRUID)

This series of products has another 128-bit chip identification number USRUID, including 96-bit user-settable identification number and 32-bit fixed identification number. The 128-bit identification code cannot be read by the memory module. USRUID can be used as a key in encryption applications, and the user program can establish a protection mechanism by detecting the key.

4.11.3 Program code protection

Support code partition protection function, each 2KBytes of APROM space is one segment, and each 1KBytes of BOOT space is one segment, and the protection status can be set through the user configuration register

4.11.4 Program CRC check

Support hardware calculation program CRC check code, the check interval can be set arbitrarily. The CRC check code is generated using the polynomial CRC16-CCITT "$X^{16}+X^{12}+X^5+1$"

4.11.5 General CRC calculation

The general CRC module can be used to verify the correctness of the program or data transmission. The check polynomial of the general CRC module is also generated using " $X^{16}+X^{12+}X^5+1$"

4.11.6 Illegal memory access detection

If you access an illegal memory address in the ARM microcontroller, the bus system will respond with an error signal, which can provide a better method of program error detection.

4.11.7 SRAM protection function

The internal SRAM has a write protection function and can be set to partition write protection. Write protection does not affect the read function, the system register SRAMLOCK can set related functions.

4.11.8 SFR protection function

Some SFRs of key function modules have protection functions, and read and write operations are invalid in the protection state.

4.11.9 ADC test function

Confirm whether the A/D converter is operating normally by performing A/D conversion on the positive reference voltage, negative reference voltage, analog input channel, and internal reference voltage of the A/D converter.

4.11.10 GPIO pin level detection

Regardless of whether the port is configured as an output port or an input port under GPIO function mode, the pin level can be read through GPIO->DI.

5. User configuration

The user configuration area is a storage area of 128 words (512 bytes) allocated in FLASH. The following functions can be set through the configuration area register:

- LVR reset voltage.
- Power-on reset startup space (APROM/BOOT) .
- User program, user UID, Data FLASH encryption control.
- Power-on WDT enable control, initial load value.
- SWD debugging function.
- External reset function and pin assignment.

6. Electrical characteristics

6.1 MCU absolute maximum ratings

symbol	parameter	Min	Max	Unit
V_{DD}-V_{SS}	power source voltage	-0.3	5.8	V
V_{IN}	input voltage	VSS-0.3	VDD+0.3	V
T_A	operating temperature	-40	+105	℃
T_{ST}	Storage temperature	-55	+150	℃
I_{DD}	VDD maximum input current	-	120	mA
I_{SS}	VSS maximum output current	-	120	mA
I_{IO}	Maximum sink current of a single I/O	-	50	mA
	Maximum source current of a single I/O	-	40	mA
	Maximum sink current of all I/Os	-	100	mA
	Maximum source current of all I/Os	-	100	mA

6.2 MCU DC electrical parameter

(V_{DD}-V_{SS}=2.1~5.5V, T_A=25℃)

symbol	parameter	test condition	Min	Typ	Max	Unit
V_{DD}	operating voltage	HCLK=64MHz	2.1	-	5.5	V
I_{DD1}	operating current	HCLK=64MHz,HSI=64MHz, ALL APBCLK OFF,V_{DD}=5.0V	-	14	-	mA
I_{DD2}		HCLK=64MHz,HSI=64MHz, ALL APBCLK OFF,V_{DD}=3.3V	-	14	-	mA
I_{DD3}		HCLK=48MHz,HSI=48MHz, ALL APBCLK OFF,V_{DD}=5.0V	-	11	-	mA
I_{DD4}		HCLK=48MHz,HSI=48MHz, ALL APBCLK OFF,V_{DD}=3.3V	-	11	-	mA
I_{DD5}		HCLK=40KHz,LSI=40KHz, ALL APBCLK OFF,V_{DD}=5V	-	0.28	-	mA
I_{DD6}		HCLK=40KHz,LSI=40KHz, ALL APBCLK OFF,V_{DD}=3.3V	-	0.28	-	mA
I_{DEEP_SLEEP}	Deep sleep mode current	(LDODS=0) LDO actiavte, V_{DD}=5V	-	200	-	uA
		(LDODS=1) LDO at low power consumption mode V_{DD}=5V	-	5	-	uA
I_{SLEEP}	Sleep mode current	LDO at low power consumption mode V_{DD}=5V	-	5	-	uA
V_{IL}	input low level	-	VSS	-	0.3VDD	V
V_{IH}	input high level	-	0.7VDD	-	VDD	V
I_{OL1}	Low output current	V_{DD}=5V GPIOxDR[n]=0 VIO=1.5V	-	-	50	mA
I_{OL2}	Low output current	V_{DD}=5V GPIOxDR[n]=1 VIO=1.5V	-	-	25	mA
I_{OH1}	high output current	V_{DD}=5V GPIOxDR[n]=0 VIO=3.5V	-	-	40	mA
I_{OH2}	high output current	V_{DD}=5V GPIOxDR[n]=1 VIO=3.5V	-	-	20	mA
R_{UP}	Pull-up resistor	-	-	33	-	KΩ
R_D	Pull-down resistor	-	-	33	-	KΩ
F_{AHBCLK}	AHB clock	-	-	-	64	MHz
F_{APBCLK}	APB clock	-	-	-	64	MHz

6.3 MCU AC electrical parameter

6.3.1 Power-on reset time

symbol	parameter	test condition	Min	Typ	Max	Unit
T_{RESET}	Reset time	VDD=5V	-	4.5	-	ms
T_{VDDR}	VDD rise rate	VDD=5V	2	-	-	us/V
T_{VDDF}	VDD fall rate	VDD=5V	2	-	-	us/V

6.3.2 Internal high-speed oscillator (HSI)

symbol	parameter	Min	Typ	Max	Unit
V_{HSI}	operating voltage	2.1	-	5.5	V
T_A	operating temperature	-40	-	105	℃
I_{HSI}	operating current V_{DD}=5.0V,T_A=25℃	-	300	-	uA
F_{HSI48M}	T_A=25℃,V_{DD}=5.0V	-	48	-	MHz
	T_A=25℃,V_{DD}=2.1~5.5V	-0.5	-	+0.5	%
	T_A=0℃~85℃,V_{DD}=2.1~5.5V	-1.5	-	+1.0	%
	T_A=-40℃~105℃,V_{DD}=2.1~5.5V	-2.0	-	+1.0	%
F_{HSI64M}	T_A=25℃,V_{DD}=5.0V	-	64	-	MHz
	T_A=25℃,V_{DD}=2.1~5.5V	-0.5	-	+0.5	%
	T_A=0℃~85℃,V_{DD}=2.1~5.5V	-2.0	-	+1.0	%
	T_A=-40℃~105℃,V_{DD}=2.1~5.5V	-2.5	-	+1.0	%

6.3.3 Internal low-speed oscillator (LSI)

symbol	parameter	Min	Typ	Max	Unit
V_{LSI}	operating voltage	2.1	-	5.5	V
T_A	operating temperature	-40	-	105	℃
I_{LSI}	operating current V_{DD}=5.0V,T_A=25℃	-	1	-	uA
F_{LSI}	T_A=25℃,V_{DD}=5.0V	-	40	-	KHz
	T_A=25℃,V_{DD}=2.1~5.5V	-5.0	-	+5.0	%
	T_A=-40℃~105℃,V_{DD}=2.1~5.5V	-15	-	+15	%

6.3.4 Low voltage reset (LVR)

symbol	parameter	Min	Typ	Max	Unit
V_{LVR1}	Low pressure detection threshold 1.9V	1.8	1.9	2.0	V
V_{LVR2}	Low pressure detection threshold 2.1V	2.0	2.1	2.2	V
V_{LVR3}	Low pressure detection threshold 2.6V	2.5	2.6	2.7	V

6.3.5 Low voltage detection (LVD)

symbol	parameter	Min	Typ	Max	Unit
V_{LVD1}	Low pressure detection threshold 2.0V	1.9	2.0	2.1	V
V_{LVD2}	Low pressure detection threshold 2.2V	2.1	2.2	2.3	V
V_{LVD3}	Low pressure detection threshold 2.4V	2.3	2.4	2.5	V
V_{LVD4}	Low pressure detection threshold 2.7V	2.6	2.7	2.8	V
V_{LVD5}	Low pressure detection threshold 3.0V	2.9	3.0	3.1	V
V_{LVD6}	Low pressure detection threshold 3.7V	3.6	3.7	3.8	V
V_{LVD7}	Low pressure detection threshold 4.0V	3.9	4.0	3.1	V
V_{LVD8}	Low pressure detection threshold 4.2V	4.1	4.2	4.3	V

6.4 FLASH electrical parameter

symbol	parameter	test condition	Min	Typ	Max	Unit
V_F	FLASH operating voltage	-	2.1	-	5.5	V
T_F	FLASH operating temperature	-	-40	27	125	℃
$N_{ENDURANCE}$	Number of erasing and writing	Program Flash	20000	-	-	Cycle
		Data Flash	100,000	-	-	Cycle
T_{RET}	Data retention time	25℃	100	-	-	year
T_{ERASE}	Sector erase time	-	-	4.604	-	ms
T_{PROG}	Programming time	-	-	6.25	-	us
I_{DD1}	Read current	-	-	-	3.5	mA
I_{DD2}	Programming current	-	-	-	3.5	mA
I_{DD3}	Erase current	-	-	-	2	mA

6.5 Analog circuit characteristics

6.5.1 BANDGAP electrical characteristics

VDD=2.1V-5.5V.

symbol	parameter	test condition	Min	Typ	Max	Unit
V_{REF}	Internal reference1.2V	T_A=-40℃ to 105℃	1.182	1.2	1.218	V

6.5.2 ADC0 electrical characteristics

TA＝25℃.

symbol	parameter	Min	Typ	Max	Unit
V_{AVDD}	ADC operating voltage	2.5	-	5.5	V
V_{REF}	reference voltage	-	V_{AVDD}	-	V
V_{ADI}	input voltage	0	-	V_{REF}	V
N_R	resolution	12			Bit
DNL	differential nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5us)	±2			LSB
INL	dntegral nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5us)	±4			LSB
T_{ADCK}	ADC clock period	0.5	-	-	us
T_{ADC}	ADC conversion time	-	18.5	-	T_{ADCK}
F_S	sampling Rate (V_{REF}=V_{AVDD}=5V)	100			Ksps

6.5.3 ADCB electrical characteristics

TA＝25℃.

symbol	parameter	Min	Typ	Max	Unit
V_{AVDD}	ADC operating voltage	2.5	-	5.5	V
V_{REF1}	reference voltage1	-	V_{AVDD}	-	V
V_{REF2}	reference voltage2(positiveAVREFP/ negativeAVREFN)	-	V_{AVREFP} V_{AVREFN}	-	V
V_{ADI}	Analog signal input	0	-	V_{REF}	V
N_R	resolution	12			Bit
DNL	differential nonlinearity error (T_{ADCK}=0.0156us, T_{ADC}=52*T_{ADCK})	±1.5			LSB
INL	dntegral nonlinearity error (T_{ADCK}=0.0156us, T_{ADC}=52*T_{ADCK})	±2			LSB
T_{ADCK}	ADC clock period	0.0156	-	-	us
T_{ADC}	High-speed mode single AD sampling and conversion total time (sampling time=13.5*T_{ADCK})	-	52	-	T_{ADCK}
F_C	Conversion rate	1.4			Msps
F_S	sampling Rate	1.2			Msps

Note: Does not include quantization error.

6.5.4 OP0/1 electrical parameter

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, V_{IN+}=1V, Unless otherwise indicated.

symbol	parameter	condition	Min	Typ	Max	Unit
VDD	power source voltage	-	2.5	-	5.5	V
I_Q	static current	V_{SENSE}=0mV	-	2.4	3.8	mA
I_{SD}	shutdown current	-	-	20	-	nA
T_A	operating temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input offset voltage	Not zeroed	-	±3.0	-	mV
		zeroed	-	±0.5	-	
V_{CM}	Common mode input voltage range	-40℃~105℃	0	-	VDD-1.3	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
Output characteristics						
C_{LOAD}	Capacitive load	-	-	100	-	pF
V_{OH}	Maximum output voltage	-40℃~105℃,I_{LOAD}=1mA	-	-	VDD-0.1	V
		-40℃~105℃,I_{LOAD}=5mA	-	-	VDD-0.3	
		-40℃~105℃,I_{LOAD}=10mA	-	-	VDD-0.5	
V_{OL}	Minimum output voltage	-40℃~105℃,I_{LOAD}=1mA	0.1	-	-	V
		-40℃~105℃,I_{LOAD}=5mA	0.3	-	-	
		-40℃~105℃,I_{LOAD}=10mA	0.5	-	-	
Frequency characteristics						
A_{OL}	Open loop gain	-	-	90	-	dB
BW	Bandwidth	C_{LOAD}=100pF	10	-	-	MHz
PSRR	Power supply rejection ratio	VDD=2.5~5.5V, V_{IN+}=1V,V_{SENSE}=0mV	-	80	-	dB
CMRR	Common mode rejection ratio	V_{IN+}=0.3V~(VDD-1.3V) -40℃~105℃	-	100	-	dB
Transient characteristics						
SR	Slew rate	C_{LOAD}=100pF	±10	±15	-	V/μs
T_{STB}	stable time	-	-	-	1.5	μs

6.5.5 ACMP0/1 electrical parameter

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, V_{IN+}=1V, Unless otherwise indicated.

symbol	parameter	condition	Min	Typ	Max	Unit
VDD	power source voltage	-	2.1	-	5.5	V
I_Q	static current	V_{SENSE}=0.1V	-	0.1	0.2	mA
I_{SD}	shutdown current	V_{SENSE}=0.1V	-	10	-	nA
T_A	operating temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input offset voltage	Not zeroed	-	±4.0	-	mV
		zeroed	-	±0.5	-	
V_{CM}	Common mode input voltage range	-40℃~105℃	-0.1	-	VDD-1.3	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
V_{HYS}	Input hysteresis voltage	VDD=2.1~5.5V, V_{IN+}=0.5V	-	0 ±10 ±20 ±60	-	mV
Output characteristics						
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	VDD	V
V_{OL}	Minimum output voltage	-40℃~105℃	0	-	-	V
Frequency characteristics						
A_{OL}	Open loop gain	-	-	90	-	dB
BW	Bandwidth	-	-	200	-	MHz
PSRR	Power supply rejection ratio	VDD=2.1~5.5V,V_{IN+}=1V, V_{SENSE}=0mV	-	80	-	dB
CMRR	Common mode rejection ratio	VDD=2.1~5.5V, -40℃~105℃	-	100	-	dB
Transient characteristics						
T_{STB}	stable time	-	-	-	1.5	μs
T_{PGD}	Response delay	V_{COM}=1V, V_{IN+}= V_{IN-} ±0.1V	-	50	100	ns

6.5.6 PGA0/1 electrical parameter

T_A=25℃, VDD=5V, V_{IN+}=0.1V, Unless otherwise indicated. (G is gain)

symbol	parameter	condition	Min	Typ	Max	Unit
VDD	power source voltage	-	2.5	-	5.5	V
I_Q	static current	V_{OUT}=2V	-	2.1	3.3	mA
I_{SD}	shutdown current	-	-	20	-	nA
T_A	operating temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input offset voltage	-	-	±2.5	-	mV
V_{CM}	Common mode input voltage range	-40℃~105℃	0.07*VDD/ G	-	0.93*VDD/ G	V
I_B	Input bias current	-	-	10	-	pA
I_{OS}	Input offset current	-	-	10	-	pA
Output characteristics						
EG	Gain error	G=4,8	-1	-	1	%
		G=10,12,14,16	-2	-	2	
		G=32	-3	-	3	
C_{LOAD}	Capacitive load	-	-	30	-	pF
V_{OH}	Maximum output voltage (A0O、A1O)	-40℃~105℃,I_{LOAD}=5mA	-	-	VDD-0.5	V
V_{OL}	Minimum output voltage (A0O、A1O)	-40℃~105℃,I_{LOAD}=5mA	0.5	-	-	V
Frequency characteristics						
BW	Bandwidth	R_{LOAD}=0.8MΩ, C_{LOAD}=3pF,G=4	-	2	-	MHz
PSRR	Power supply rejection ratio	VDD=2.5~5.5V	-	70	-	dB
CMRR	Common mode rejection ratio	-40℃~105℃	-	80	-	dB
Transient characteristics						
SR	Slew rate	G=10, C_{LOAD}=10pF	6	10	-	V/μs
T_{STB}	stable time	-	-	-	2	μs

6.5.7 Temperature sensor electrical parameter

VDD=5V.

symbol	parameter	test condition	Min	Typ	Max	Unit
T_{LINE}	Linearity	-	-	±4	-	℃
K_{AVG}	slope	-40℃~105℃	3.3	3.5	3.7	mV/℃
V_{25}	25℃ output voltage	T_A=25℃	0.99	1	1.01	V
T_S	Setup time	-	-	-	10	μs
T_{SMP}	ADC sampling time	-	150	-	-	μs

6.6 GATE DRIVER (6N) electrical characteristics (CMS32M5733)

6.6.1 Static electrical characteristics parameter

(Unless otherwise indicated, V_{GVDD}-V_{PGND}=15V, T_A=25℃) .

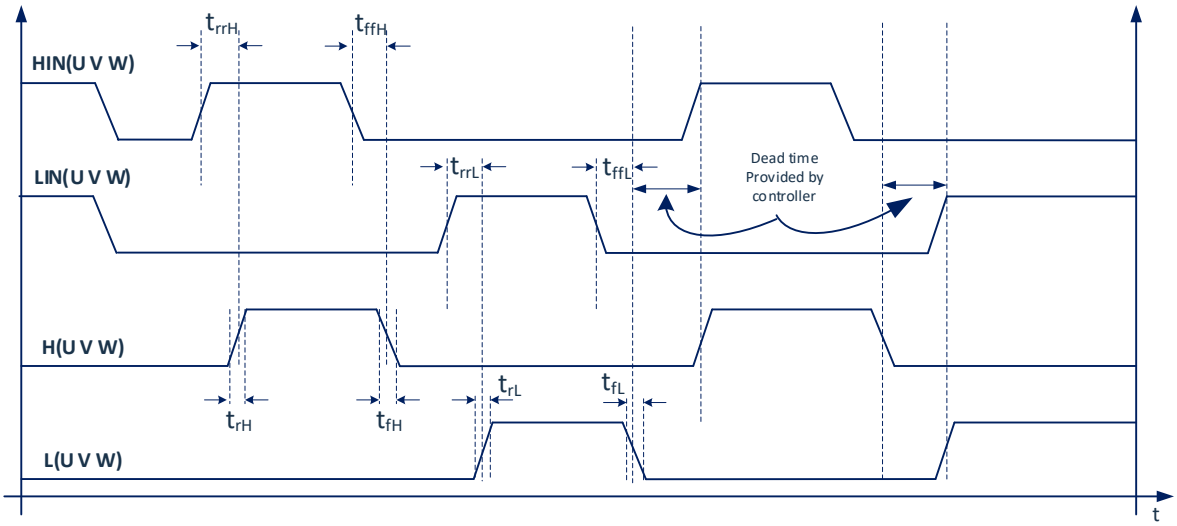
symbol	parameter	test condition	Min	Typ	Max	Unit
V_{GVDD}	operating voltage	-	5.5	-	18	V
V_{GHSx}	High-side floating voltage	-	PGND-6	-	90	V
V_{BOSTx}	High-side bootstrap power supply	-	V_{GHSx}+5.5	-	V_{GHSx}+18	V
V_{GHx}	High-side output voltage	-	V_{GHSx}	-	V_{BOSTx}	V
I_{GVDD}	static current	-	210	330	450	uA
I_{GVDDop}	operating current	f_{LINx}=20kHz, f_{HINx}=20kHz	-	1500	-	uA
V_{INH}	input high level	-	2.5	-	5.5	V
V_{INL}	input low level	-	-	-	0.8	V
	Input pull-down resistance	-	-	110	-	KΩ
Isource	Peak current drawn by output	V_{GHx}=V_{GHSx}=0V, V_{GLx}=0V	-	1.2	-	A
Isink	Output sinks peak current	V_{GHx}=V_{BOSTx}=15V, V_{GLx}=V_{GVDD}=15V	-	2	-	A
V_{GHSNx}	GHSx negative pressure	V^{BOSTx}=15V	-	-8	-	V

6.6.2 Dynamic electrical characteristics parameter

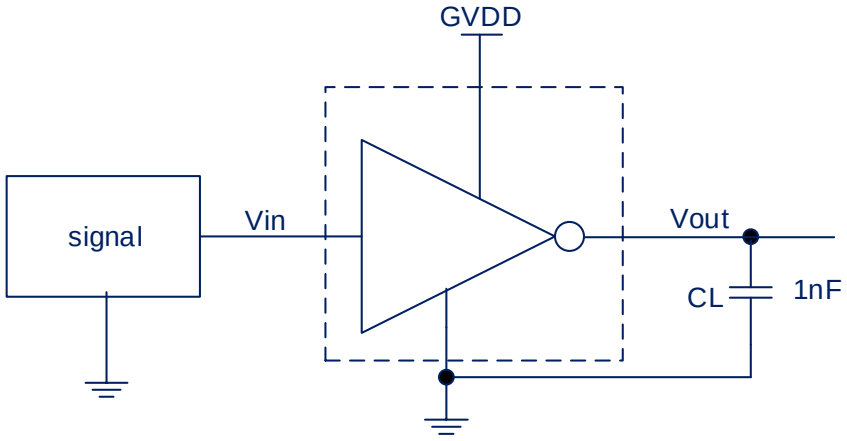
(Unless otherwise indicated, V_{GVDD}-V_{PGND}=15V, TA=25℃, C_{load}=1nF)

parameter	symbol	test condition	Min	Typ	Max	Unit
Turn on transmission delay time	Ton	Signal frequency 10KHz, V_{GHSx}=0V	-	120	200	ns
Turn-off transmission delay time	toff		-	120	200	
Turn-on rise time	tr		-	37	-	
Turn off fall time	tf		-	30	-	
Dead time	DT	No additional dead zone	300	500	700	
Dead zone matching time (6 channels)	MDT	No additional dead zone	-	-	50	
Delay matching data (6 channels)	MT	Extra DT>1us	-	-	50	
Output pulse width matching	PM	Extra DT>1us, PWin=10us, PM=PWout-PWin	-	-	50	

6.6.3 Time parameter test



Schematic diagram of the input and output logic relationship and time parameter of the half-bridge driver



Test circuit

6.7 GATE DRIVER (6N) electrical characteristics (CMS32M5736)

6.7.1 Absolute maximum ratings

(T_A=25℃, unless otherwise specified, all pins take GND as the reference point)

parameter	symbol	Value	Unit
High-side floating offset absolute voltage	$V_{B1,2,3}$	225	V
High-side floating offset relative voltage	$V_{S1,2,3}$	$V_{B1,2,3}$-25~$V_{B1,2,3}$	V
High-side output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$~$V_{B1,2,3}$	V
Maximum power source voltage	V_{CC}	25	V
Low-side output voltage	$V_{LO1,2,3}$	V_{CC}	V
Maximum input voltage (HIN1,2,3/LIN1,2,3)	V_{IN}	10	V
Maximum offset voltage Slew rate	dV_S/dt	50	V/ns
Maximum power consumption (note 1)	P_D	1.25	W
Junction to ambient thermal resistance	θ_{JA}	100	℃/W
Junction temperature	T_J	150	℃
Storage temperature	T_S	-55~+150	℃
Pin soldering temperature (duration 10s)	T_L	260	℃
ESD(note 2)		2000	V

Note:

1) In any case, do not exceed PD, The maximum power consumption calculation formula under different ambient temperature is : $P_D=(150℃-T_A)/\theta_{JA}$

$T_A$is the ambient temperature of the circuit, θ_{JA} is the thermal resistance of the package, 150℃is the maximum operating junction temperature of the circuit;

2) Human body model, the "100pF" capacitor is discharged through the "1.5KΩ" resistor;

3) When the circuit working condition exceeds the range specified by the absolute maximum rating, it is very likely to cause immediate damage to the circuit

6.7.2 Recomanded operating condition

(T_A=25℃, unless otherwise specified, all pins take GND as the reference point)

parameter	symbol	Min	Typ	Max	Unit
Power source voltage	V_{CC}	8	15	20	V
High-side floating offset absolute voltage	$V_{B1,2,3}$	$V_{S1,2,3}$+8	$V_{S1,2,3}$+15	$V_{S1,2,3}$ + 20	V
High-side floating offset relative voltage	$V_{S1,2,3}$	GND-5	-	200	V
High-side output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{S1,2,3}$+15	$V_{B1,2,3}$	V
Low-side output voltage	$V_{LO1,2,3}$	0	15	V_{CC}	V
input voltage (HIN1,2,3 /LIN1,2,3)	V_{IN}	0	-	5	V
operating temperature range(note 1)	T_{opr}	-20	-	+85	℃

Note:

1) T_{opr} indicates the ambient temperature of circuit operation;

2) Working outside the recommended conditions for a long time may affect its reliability. It is not recommended that the chip work longer than the recommended conditions.

6.7.3 Electrical characteristics parameter table

(T_A=25℃, V_{CC}=$V_{BS1,2,3}$=15V, $V_{s1,2,3}$=GND unless otherwise indicated)

parameter	symbol	test condition	Min	Typ	Max	Unit
Power source current parameter						
V_{CC} static current	I_{VCCQ}	$V_{HIN1,2,3}$=$V_{LIN1,2,3}$=0	200	330	460	μA
V_{BS} static current	I_{VBSQ}	$V_{HIN1,2,3}$=0	33	55	75	μA
V_{CC} dynamic current	I_{VCCD}	$f_{LIN1,2,3}$=20kHz	-	430	-	μA
V_{BS} dynamic current	I_{VBSD}	$f_{HIN1,2,3}$=20kHz	-	180	-	μA
V_B Floating power supply leakage current	I_{VSLK}	V_B=V_S=200V	-	-	0.1	μA
power source voltage parameter						
V_{CC} undervoltage high level potential	V_{CCHY+}		6.5	7	7.5	V
V_{CC} undervoltage high level potential	V_{CCHY-}		5.8	6.3	6.8	V
V_{CC} undervoltage hysteresis level	V_{CCHY}		0.4	0.7	-	V
V_{BS} undervoltage high level potential	V_{BSHY+}		6.5	7	7.5	V
V_{BS} undervoltage high level potential	V_{BSHY-}		5.8	6.3	6.8	V
V_{BS} undervoltage hysteresis level	V_{BSHY}		0.4	0.7	-	V
V_S static negative pressure	V_{SQN}		-	-8.0	-	V
Input parameter						
input high level current	I_{IN+}	V_{HIN} or V_{LIN}=5V	-	60	90	μA
input low level current	I_{IN-}	V_{HIN} or V_{LIN}=0	-	0	1	μA
input high level potential	V_{IN+}		2.6	-	-	V
input low level potential	V_{IN-}		-	-	0.8	V
Input hysteresis level	V_{INHY}		-	1.2	-	V
Output parameter						
High level short circuit pulse current	I_{OUT+}	V_{HIN} or V_{LIN}=5V V_{HO} or V_{LO}=0 PWD≤10μs	0.8	1.1	1.4	A
Low-level short-circuit pulse current	I_{OUT-}	V_{HIN} or V_{LIN}=0 V_{HO} or V_{LO}=15V PWD≤10μs	1.5	2.0	2.5	A
High level output voltage	V_{OUT+}	I_{OUT}=100mA	-	0.52	0.8	V
Low-level output voltage	V_{OUT-}	I_{OUT}=100mA	-	0.23	0.35	V
Time parameter						
Output rising edge transmission time	T_{ON}	NO Load	-	260	390	ns

Output falling edge transmission time	T_{OFF}	NO Load	-	260	390	ns
Output rise time	T_{rise}	C_L=3.3nF	-	60	90	ns
Output fall time	T_{fall}	C_L=3.3nF	-	33	50	ns
Dead time	DT	NO Load	150	300	450	ns
High and low side matching time	MT	ΔT_{ON} & ΔT_{OFF}	-	-	50	ns

6.8 EMC characteristic

6.8.1 EFT characteristics

symbol	parameter	test condition	Level
V_{EFTB}	Fast transient voltage burst limits to beapplied through 0.1uF(capacitance) on VDDand VSSpins to induce a functional disturbance	T_A = + 25℃, HSI=64MHz, conforms to IEC 61000-4-4	4B

Note：Electrical fast transient (EFT) immunity performance is closely related to system design (including power supply structure, circuit design, layout, chip configuration, program structure, etc.). The EFTparameter in the above table is the result measured on the CMS internal test platform, and is not suitable for all application environments. The test data is only for reference. All aspects of system design may affect EFT performance. In applications with high EFT performance requirements, attention should be paid to avoid interference sources affecting system operation when designing. It is recommended to analyze interference paths and optimize the design to achieve the best anti-interference performance.

6.8.2 ESD characteristics

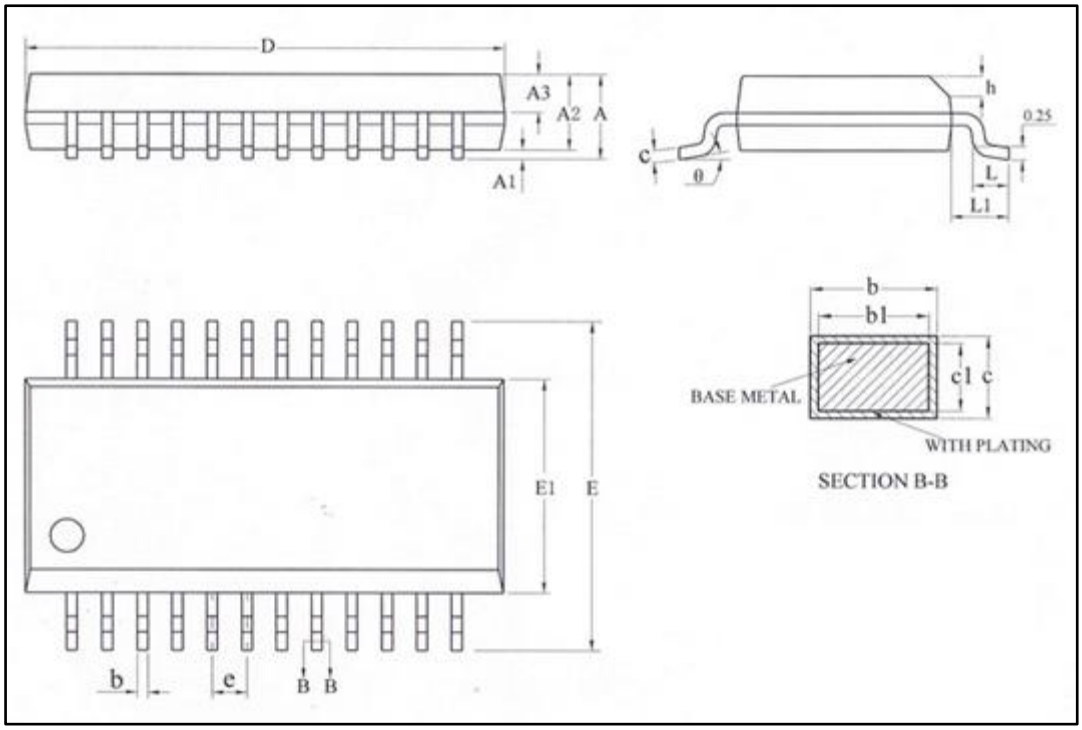
symbol	parameter	test condition	Level
V_{ESD}	Electrostatic discharge (human body discharge mode HBM)	T_A = + 25℃, JEDEC EIA/JESD22- A114	3B
	Electrostatic discharge (machine discharge modeMM)	T_A = + 25℃, JEDEC EIA/JESD22- A115	C

6.8.3 Latch-Up characteristics

symbol	parameter	test condition	Test type
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Level Class I (TA = +25℃)

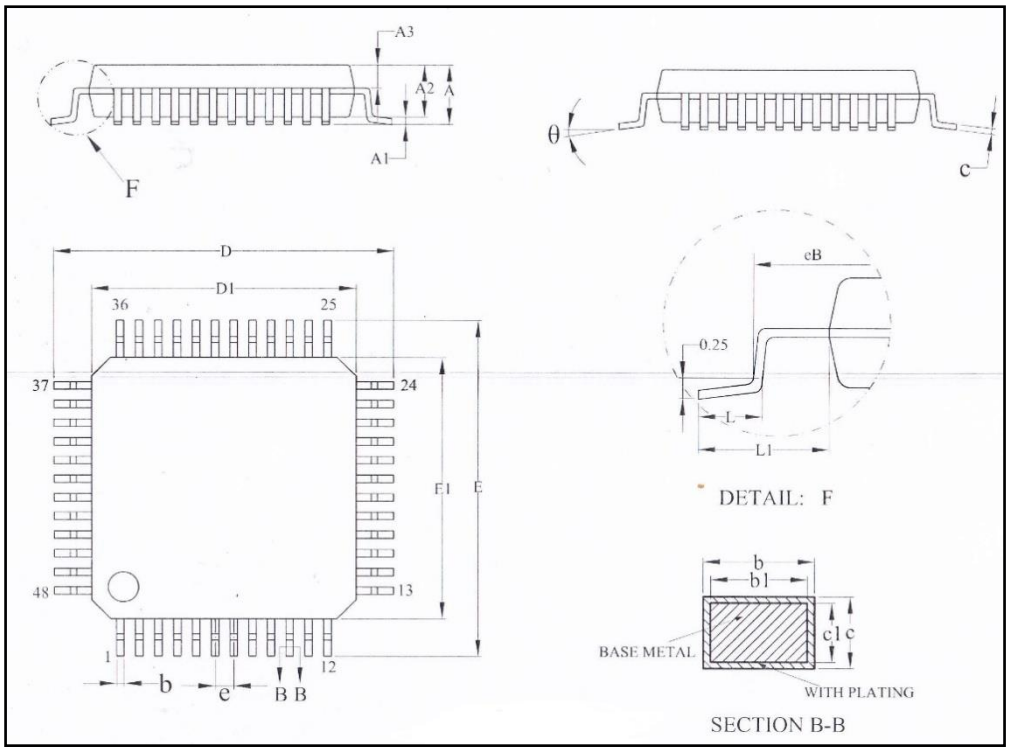
7. Package size

7.1 SSOP24



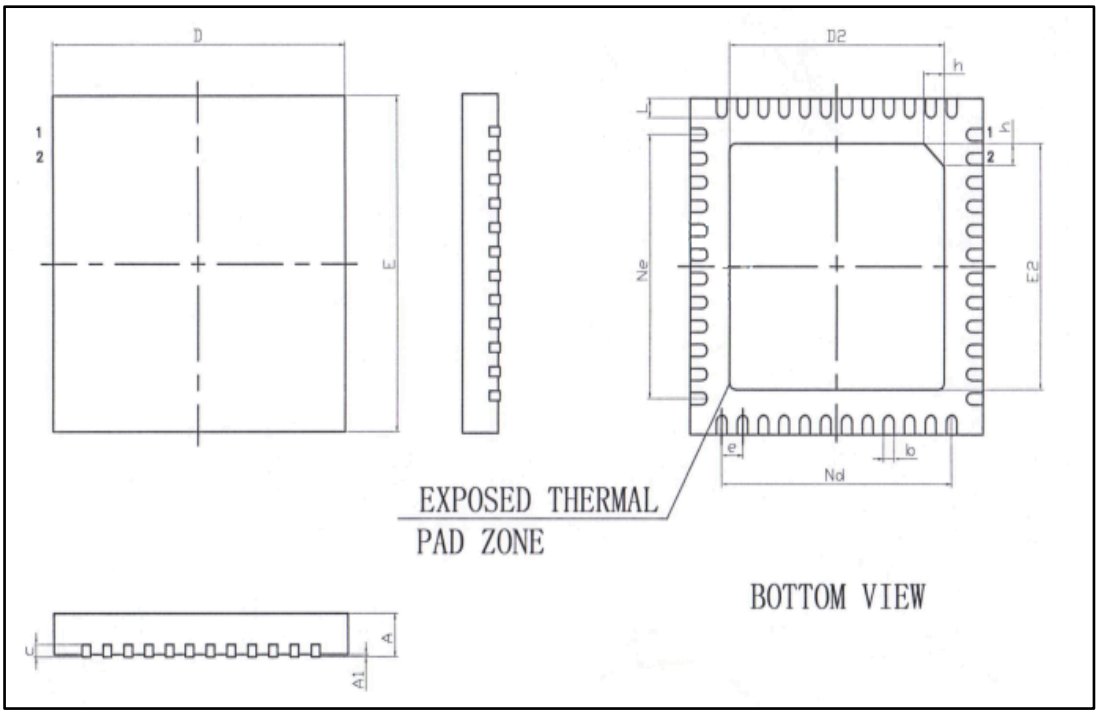
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

7.2 LQFP48



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

7.3 QFN48



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Nd	4.40BSC		
Ne	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

8. Ordering Information

Product number	core	main (MHz)	Program FLASH(KB)	Data FLASH(KB)	SRAM(KB)	Built-in drive	Built-in LDO	Hardware multiplier	Hardware divider	GPIO	12-Bit ADC0	12-Bit ADCB	Built-in op amp	Built-in PGA	Built-in comparator	EPWM	CCP	timer	UART	I2C	SPI	Temperature Sensor	CRC	WDT	WWDT	PACKAGE
CMS32M5710L048	M0	64	64	1	8	-	0	1	1	46	12	12	2	2	2	6	2	4	2	1	1	1	1	1	1	LQFP48
CMS32M5733Q048	M0	64	64	1	8	6N (90V)	0	1	1	32	11	12	2	2	2	6	2	4	2	1	1	1	1	1	1	QFN48
CMS32M5736L048	M0	64	64	1	8	6N (200V)	0	1	1	32	11	12	2	2	2	6	2	4	2	1	1	1	1	1	1	LQFP48
CMS32M5736Q048	M0	64	64	1	8	6N (200V)	0	1	1	32	11	12	2	2	2	6	2	4	2	1	1	1	1	1	1	QFN48

9. Version history

Version number	time	Revised cotent
V1.00	May 2019	Original version
V1.01	Apr 2020	1) Add ADCB external reference AVREFP/AVREFN and relatives 2) Add 5710S024/5733Q048 and relatives
V1.02	Nov 2020	Add CMS32M5736 QFN048 chip information
V1.03	Jan 2021	Change CMS32M5733 and CMS32M5736 ordering information
V1.04	Feb 2023	Correct the FLASH electrical parameter
V1.0.5	Mar 2023	1) Modify 4.5.2Low voltage reset (LVR) parameters 2) Modify 6.3.4Low voltage reset (LVR) parameters
V1.0.6	Apr 2023	1) Delete 5710S024 related information description 2) Add 5736L048 related information description 3) 3.1, 3.2, 3.4 SWD function name correction 4) Modify Section6.8 EMC characteristic: Delete values and keep only levels 5) Correct 7.2 Encapsulation Information
V1.0.7	May 2023	Modified section 4.9.4